

Universal Serial Bus 4 (USB4[®]) Version 2 GEN4 Electrical Compliance Test Specification

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Acronyms

Acronym	Definition
TER	Trit Error Rate
BW	Band Width

CDR	Clock Data Recovery
DUT	Device Under Testing
NVM	Non Volatile Memory
PJ	Periodic Jitter
SSC	Spread Spectrum Clock
TJ	Total Jitter
UI	Unit Interval
UJ	Uncorrelated Jitter
UDJ	Uncorrelated Deterministic Jitter
RJ	Random Jitter
ISI	Inter Symbol Interference
DDJ	Data dependent Jitter
PPM	Parts Per Million
PRBS	Pseudo Random Bit Sequence
PRTS	Pseudo Random Trit Sequence
PAM	Pulse Amplitude Modulation
IL	Insertion Loss
RL	Return Loss

1 Introduction

- This document contains the specification of procedures, tools and criteria for electrical compliance testing of Router Assembly according to the Universal Serial Bus 4 (USB4™) Specification, Version 2.0
- USB4 v2 SigTest tool shall be used in all post-processing for Router Assembly Transmitter testing, and Receiver testing and calibration
- For guidance in operating USB4 v2 SigTest tool refer to user manual

2 Test Equipment

2.1 Overview

All equipment used for testing shall comply with the requirement lists specified below.

This includes the primary equipment that is used in the USB4 authorized test centers and may also be used by the end user for self-testing.

Other configurations and equipment may be used for self-testing as long as that equipment and the processes meet all of the stated and implied requirements and permit an equivalent level of testing.

2.2 Test Equipment Requirements

All test equipment requires calibration to ensure accurate and repeatable results. Equipment shall be calibrated prior to, and if necessary, during the test procedure.

2.2.1 Test Point Access Boards

To gain access to the required signals, a variety of test point access boards are required. Test Point Access boards provide test points for the pins on the USB4 USB Type-C connector and an easy way to control the DUT.

Recommended Test Equipment:

1. Certified USB4 Plug and Receptacle Test fixtures
2. Certified USB4 Micro-Controller Test Module with USB cable
3. Control PC \ Scope running the latest USB4 SW Electrical Test Tool (ETT)

2.2.2 Real Time Scopes

Required Test Equipment Capabilities:

- DC to 25GHz at -3db bandwidth or higher
- Sampling rate $\geq 80\text{Gs/s}$
- Sample clock jitter/intrinsic jitter $< 100\text{fs rms}$ within the acquired time range of 10 to 50 $\mu\text{sec/div}$
- Intrinsic vertical noise $< 3\text{mV rms}$ within the acquired voltage range of 10 to 100mV/div
- SNDR $\geq 38.5\text{dB}$ measured using common test methodology for ADC, by applying high quality/low noise sine-wave (3 sine-wave test frequencies: 6,10,12.8GHz, magnitude 800mV p-p differential) at Scope input and measuring the output signal-to-noise-and-distortion ratio while compensating scope intrinsic noise as defined by USB4v2 standard

2.2.3 Pattern Generator

Generate USB4 signal with a variety of patterns, jitter injection capability.

Required Test Equipment Capabilities:

- Data rates $\geq 25.6\text{Gbps}$

- BERT intrinsic SNDR > 39dB
- BERT Insertion Loss (BERT_IL, negative value) at Nyquist (12.8GHz) \geq -3dB, Nyquist/2 (6.4GHz) - Nyquist (12.8GHz) \geq 0.7dB, Nyquist/4 (3.2GHz) - Nyquist/2 (6.4GHz) \geq 0dB:

BERT Insertion Loss (IL)	Min IL (dB)	Comment
BERT_IL _{12.8GHz}	-3	IL at 12.8GHz
BERT_IL _{3.2GHz} - BERT_IL _{6.4GHz}	0	IL delta
BERT_IL _{6.4GHz} - BERT_IL _{12.8GHz}	0.7	IL delta

See section 4.1.4.1.3.2 and 4.1.4.1.3.3 of this document for measurement procedure

- Data patterns: PAM2 PRBS11, PAM3 PRTS7 and PRTS19, Square waves (SQ2, SQ4, SQ16, SQ32, SQ64, SQ128, SQ256), TS2.clksw, LFPS
- Pre-coding for ternary sequences (as defined in section 4.3.2.8 of the base specification) shall be supported and enabled when needed
- Differential swing range: up to 1.2Vp-p
- Random Jitter profile no smaller than 500MHz
- Tunable 4-tap FIR, aligned with the transmitter equalization Presets defined in USB4 Base Spec Table 3-24. Minimum coefficient resolution is 0.005, while the tolerance of the normalized coefficients shall be of ± 0.007 for C[-2] and of ± 0.008 for C[-1], C[0], and C[1] coefficients per each Preset
- Glitch-free switching from PRBS11 to PRTS7 (without applying SSC downspreading) while maintaining the same jitter and noise settings
- Glitch-free switching from PRTS7 to PRTS19 with pre-coding enabled while maintaining the same jitter and noise settings
- Glitch-free switching from PRTS7 to TS2.clksw while maintaining the same jitter and noise settings
- Glitch-free switching from TS2.clksw to PRTS7 while maintaining the same jitter and noise settings
- Glitch-free switching from Electrical Idle state to LFPS, and from LFPS to Electrical Idle state
- Glitch-free SSC activation such that the SSC modulation profile starts from the generator initial frequency
- Custom clock switch profile support defined in USB4 Base Spec Table 3-26
- Frequency Variation flows Type I and II as defined in Appendix F of this document
- Glitch-free custom clock switch profile activation
- SSC spread deviation from 0.03% down to -0.34%, triangular shape
- Injection of 1 SJ source
- Common mode interference
 - Waveform: sine wave
 - Frequency: 100-500MHz
 - Amplitude: 10-200mV
- Differential mode interference
 - Waveform: sine wave
 - Frequency: 10GHz \pm 100MHz
 - Amplitude: 10-100mV p-p
- Error insertion with variable TER symbol error ratio (1E-4, 1E-6, ...)

Note: "Glitch-free" definition is same TX clock usage during PRBS, PRTS, TS2.CLKSW transitions without any change. In addition, transition from sending PRBS11 to PRTS7, PRTS7 to TS2.CLKSW, TS2.CLKSW to PRTS7 shall be continuous (right after PRBS11 data ends PRTS7 data starts w/o any gap or overlap, same for other pattern switches)

2.2.4 Network Analyzer

Required Test Equipment Capabilities:

- 2 ports used simultaneously
- 10MHz–20GHz bandwidth
- Dynamic range > 50db
- Time domain option
- The de-embedding files (s4p) shall be up to 20GHz

2.2.5 RF Signal Generator

Required Test Equipment Capabilities:

- Differential ¼ Rate Clock at 6.4GHz (Phase matched balun can be used to convert single ended signal to differential)
- Tunable Output Power with sufficient output amplitude to meet calibration targets of aggressors as defined in Appendix A.2.3
- Output DC coupled

2.2.6 Accessories

2.2.6.1 Low Insertion Loss Phase Matched Cable:

Required Test Equipment Capabilities for 1m RF cable:

- Phase matched max of $\pm 5^\circ$ @ 40GHz
- Max IL in 10GHz < 1.5dB

Note: Any length of cable is permitted up to 1m unless written otherwise.

2.2.6.2 ISI Channel

Required Test Equipment Capabilities:

PCB coupons with various insertion losses of 2–8dB @12.8GHz

2.2.6.3 DC Block

Required Test Equipment Capabilities:

- DC Blocks with bandwidth ≥ 40 GHz
- Insertion Loss < 1dB up to 40GHz
- Capacitance of 135nF–265nF (220nF is recommended)

2.2.6.4 Power Splitter

Required Test Equipment Capabilities:

- Bandwidth ≥ 18 GHz

- Insertion Loss specification shall be selected to meet the calibration targets defined in section A.2.5 of this document

2.2.6.5 USB4 Passive and LRD Cables

- USB Type-C GEN3 certified passive cable (while Insertion Loss Fit (ILfit) target shall be -7.5 @ 10GHz and -9.5dB @ 12.8GHz with tolerance range of [-0 : + 1] and [-0 : + 1.5]dB respectively per every physical lane pair being used for receiver testing)
- The passive cable shall be e-marked
- USB4 Active cable. The Active cable shall be e-marked
- USB4 LRD cable. The LRD cable shall be e-marked

2.2.6.6 Termination

Required Test Equipment Capabilities:

- Impedance 50Ω nominal
- Frequency DC to 20GHz

3 Router Assembly Transmitter Testing

- Router Assembly transmitter compliance testing is defined at the output of a compliance plug fixture referenced to TP2 compliance point.
- Calibration shall be applied in cases where direct measurement is not feasible.

The following sections provide detailed information on the setup and testing of the USB4 GEN4 parameters. In the event of a discrepancy, the USB4 2.0 Specification prevails.

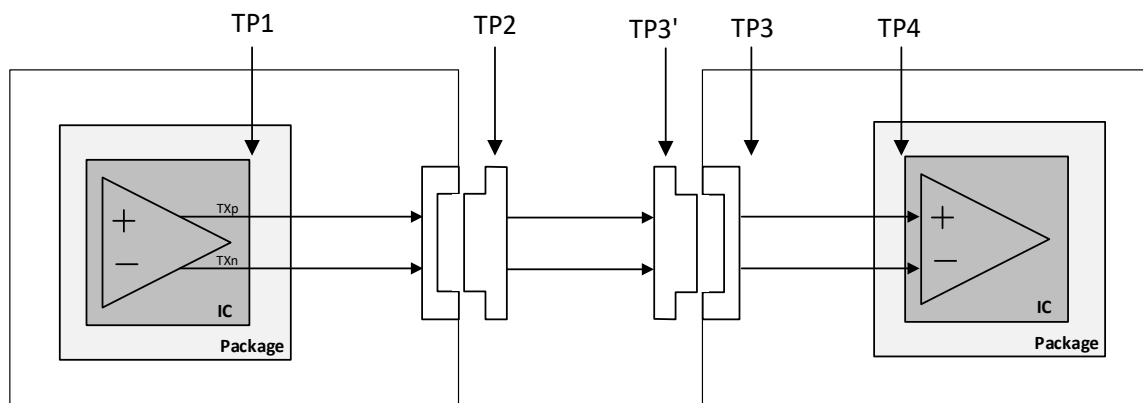


Figure 1. USB4 TX Compliance Points Definition

3.1 Transmitter Test Setup

Figure #2 illustrates the connections to the DUT and control PC used for Transmitter testing. Cable assembly connecting DUT to Oscilloscope shall be measured using Network analyzer for further de-embedding in SigTest tool

Note:

1. Use Oscilloscope requested **Analog** Bandwidth. In case Digital Filter is used to set requested Oscilloscope Bandwidth, the usage of Brick-Wall Filter is **not** recommended
2. Before beginning any test or data acquisition, the Oscilloscope must be warmed, and calibrated. Signal vertical scaling must be optimized for maximum opening cross all tests (at least 80% of maximum scope vertical range)

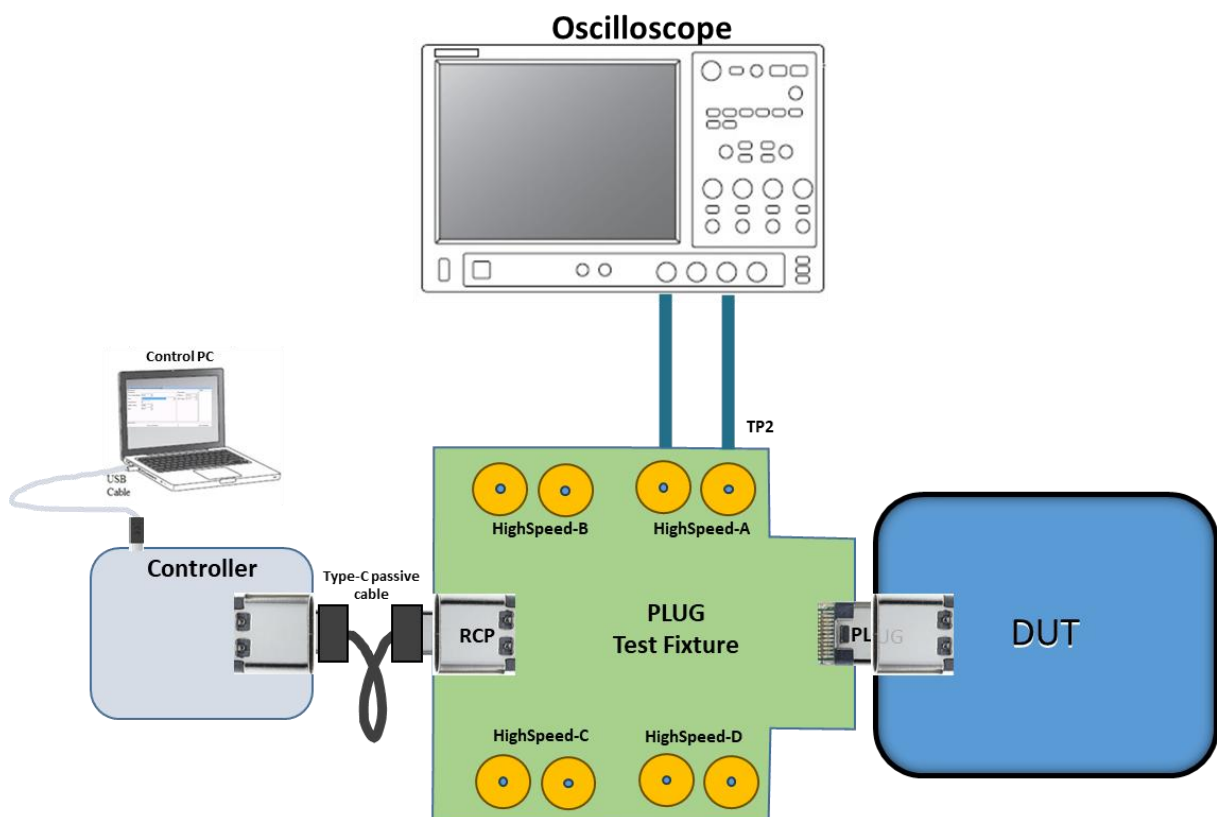


Figure 2. Transmitter TP2 Test Setup

3.2 Connecting to the DUT

1. Connect Lane under test TX_P, TX_N to the Oscilloscope.
2. Connect the Low speed signals from the USB4 test Fixture to the USB4 Micro-controller port using a USB Type-C passive cable.
3. The USB4 Micro-controller is connected to Control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT).

3.3 GEN4 Router Assembly Transmitter Compliance

Note: Refer to Sections 3.2.3

3.3.1 GEN4 Transmitter Equalization

3.3.1.1 Reference

USB4 Specification Section 3.2.3.8, Table 3-24

Preset Number	C[-2]	C[-1]	C[0]	C[1]
0	0	0	1	0
1	0	0	0.95	-0.05
2	0	0	0.9	-0.1
3	0	0	0.85	-0.15
4	0	-0.05	0.95	0
5	0	-0.05	0.9	-0.05
6	0	-0.05	0.85	-0.1
7	0	-0.05	0.8	-0.15
8	0	-0.1	0.9	0
9	0	-0.1	0.85	-0.05
10	0	-0.1	0.8	-0.1
11	0	-0.1	0.75	-0.15
12	0	-0.15	0.85	0
13	0	-0.15	0.8	-0.05
14	0	-0.15	0.75	-0.1
15	0	-0.15	0.7	-0.15
16	0.025	-0.15	0.825	0
17	0.025	-0.15	0.775	-0.05
18	0.025	-0.15	0.725	-0.1
19	0.025	-0.15	0.675	-0.15
20	0	-0.2	0.8	0
21	0	-0.2	0.75	-0.05
22	0	-0.2	0.7	-0.1
23	0	-0.2	0.65	-0.15
24	0.025	-0.2	0.775	0
25	0.025	-0.2	0.725	-0.05
26	0.025	-0.2	0.675	-0.1
27	0.025	-0.2	0.625	-0.15
28	0.05	-0.2	0.75	0
29	0.05	-0.2	0.7	-0.05
30	0.05	-0.2	0.65	-0.1
31	0.05	-0.2	0.6	-0.15
32	0	-0.25	0.75	0
33	0	-0.25	0.7	-0.05
34	0.025	-0.25	0.725	0
35	0.025	-0.25	0.675	-0.05
36	0.05	-0.25	0.7	0
37	0.05	-0.25	0.65	-0.05

38	0.075	-0.25	0.675	0
39	0.075	-0.25	0.625	-0.05
40	0	-0.1	0.4	0
41	0	0	0.5	0

Transmit Equalization Presets Table

3.3.1.2 Requirement

For low swing mode (presets 40-41 only) the transmitter swing attenuation requirement is $6 \pm 1\text{dB}$

For both low and full swing modes the tolerance of the normalized coefficients shall be of ± 0.015 for $C[-2]$ and of ± 0.025 for $C[-1]$, $C[0]$, and $C[1]$ coefficients

3.3.1.3 Test Objective

Confirm that the transmitter equalization presets are within the USB4 2.0 Specification limits

3.3.1.4 Test Method

- Speed GEN4. Lane under test pattern PRTS7, remaining lanes shall be activated as aggressors transmitting PRTS19 with preset#0 to 50Ω termination. SSC shall be enabled during the test
- Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
- Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
- Capture the differential output signal with all presets one by one (total 42 waveforms). Record the Oscilloscope vertical scaling setting (voltage/div) for each preset, it will be used for further scope intrinsic noise measurement as described in Appendix C of this document
 - Preset0 is used as a reference preset for other presets analysis. Make sure to capture Preset0 and analyzed Presets at the same DUT TX conditions without power cycling in-between
- Run SigTest tool according to User Manual documentation (refer to section 6.2.1)
- Check SigTest report for pass/fail status. All presets must be passing
- Repeat the test for all remaining USB4 Transmitter Lanes
 - In case that more than one Oscilloscope differential channel pair is used, repeat the Oscilloscope vertical scale tuning (voltage/div) and recording for each preset

Note: The de-embedding of the cable assembly connecting TP2 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed (See Appendix B for correct Network Analyzer setup)

3.3.2 GEN4 Transmitter Timing and Voltage measurement subsets

3.3.2.1 Reference

USB4 Specification section 3.2.3 Table 3-22.

3.3.2.2 Requirement

Subset type	Symbol	Min	Max	Units
Timing Parameters subset	UI	39.0508	39.0742	ps
	SSC_DOWN_SPREAD_RANGE	0.2	0.3	%
	SSC_DOWN_SPREAD_RATE	30	33	KHz
	SSC_PHASE_DEVIATION	2.5	15.5	ns pp
	SSC_SLEW_RATE		500	ppm/ μ s
	UJ		0.17	UI pp
	UDJ		0.075	UI pp
	UDJ_LF		0.03	UI pp
	EVEN_ODD		0.02	UI pp
Voltage Parameters subset	V_SWING	410	545	mV p
	TX_LEVELS_MISMATCH	0.975		
	TX_SNR	34		dB
	TX_ISI_MARGIN	11		dB

3.3.2.3 Test Objective

Confirm that all listed above timing and voltage parameters are within USB4 2.0 Specification limits during steady-state

3.3.2.4 Test Method

1. Identify the preset configuration that obtains the lowest DDJ based on the Transmitter Equalization test described in section 3.3.1 of current document
2. Run SigTest tool according to User Manual documentation using corresponding preset waveform (refer to section 6.2.2). No new signal acquisition is required in this test

3. Check SigTest report for pass/fail status. All listed above timing and voltage parameters must be passing. In case only EVEN_ODD parameter fails, use PRBS11 pattern instead of PRTS7 and retest. If EVEN_ODD passes using PRBS11 then the overall result is Pass. If EVEN_ODD parameter still violates the specification limit then test Fails
4. Repeat the test for all remaining USB4 Transmitter Lanes

Note: scope intrinsic noise file shall be provided to SigTest with the same scope settings used for capturing the file with the selected preset configuration as described in Appendix C of this document

3.3.3 GEN4 Transmitter Frequency Variation Training measurement

Note: Skip this test if the Router Assembly doesn't include Re-timers

3.3.3.1 Reference

TX_FREQ_VARIATIONS_TRAINING – USB4 Specification Table 3-22.

3.3.3.2 Requirement

TX_FREQ_VARIATIONS_TRAINING:

- $-300 \leq \text{INIT_FREQ_VARIATION} \leq 300 \text{ ppm}$
- $\text{DELTA_FREQ_200ns} \leq 600 \text{ ppm}$
- $\text{DELTA_FREQ_1000ns} \leq 900 \text{ ppm}$
- $\text{FREQ_OVERSHOOT} \leq 600 \text{ ppm}$

3.3.3.3 Test Objective

Confirm that the frequency variation during Link training is within USB4 2.0 Specification limits

3.3.3.4 Test Method

1. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
2. For emulating link training set Router Assembly components as following:
 - Router shall be configured to transmit PRTS7 PAM3 pattern on all lanes. SSC modulation shall be disabled
 - Re-Timer facing USB Type-C connector shall be configured to transmit SQ224 (if supported) or SQ128 (if SQ224 is not supported) on all lanes. Re-timer shall prevent the transition to Forwarding state
3. Set Oscilloscope as following
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation to be used

- The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
 - Triggering on UI shrinkage, keep at least 10 μ s memory buffer after triggering point
4. Initiate transition to Forwarding state on the Re-Timer facing USB Type-C connector
 5. Capture the clock switch event over three stages: pre-clock switch, clock switch and post-clock switch in a single waveform as depicted in a Figure 3

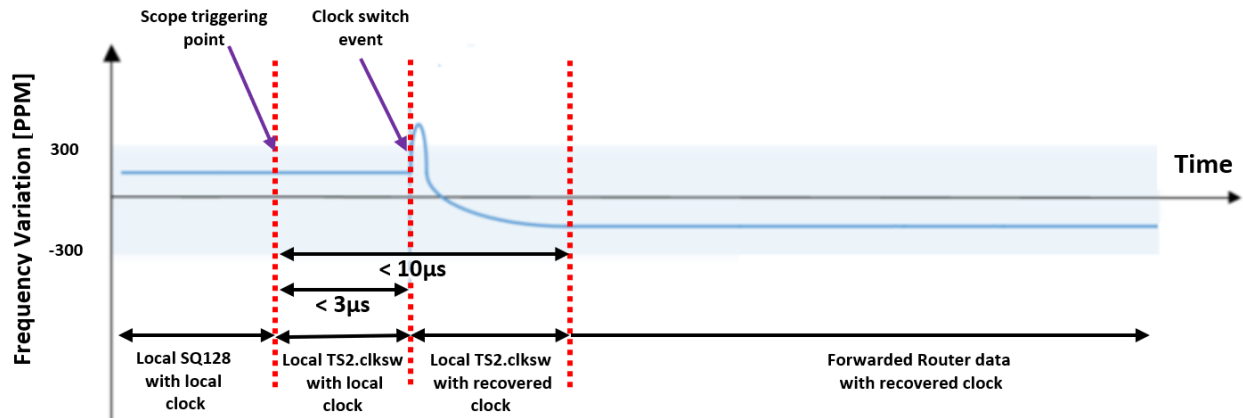


Figure 3. Frequency variation dynamics example

6. Run SigTest tool according to User Manual documentation (refer to section 6.2.3)
7. Check SigTest report for pass/fail status
8. Repeat above procedure 10 times. Use the worst case result as final
9. Repeat the test for all remaining USB4 Transmitter Lanes

Note: The de-embedding of the cable assembly connecting TP2 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed (See Appendix B for correct Network Analyzer setup)

3.3.4 GEN4 Transmitter Electrical Idle Voltage measurement

3.3.4.1 Reference

V_ELEC_IDLE - USB4 Specification section 3.2.3 Table 3-22

3.3.4.2 Requirement

$V_ELEC_IDLE \leq 20\text{mV}$.

3.3.4.3 Test Objective

Confirm that the TX peak voltage during transmit electrical idle is within USB4 2.0 Specification limits

3.3.4.4 Test Method

1. The de-embedding of the cable assembly connecting TP2 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
3. Configure DUT to Electrical Idle Mode
4. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
5. Capture the output differential signal ($V_{\text{TX-P}} - V_{\text{TX-N}}$). The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
6. Run SigTest tool according to User Manual documentation (refer to section 6.2.4)
7. Check SigTest report for pass/fail status
8. Repeat the test for all remaining USB4 lanes

3.3.5 GEN4 Transmitter AC common mode measurement

3.3.5.1 Reference

AC_CM - USB4 Specification section 3.2.3 Table 3-22

3.3.5.2 Requirement

$AC_CM \leq 100mVp-p$

3.3.5.3 Test Objective

Confirm that the transmitter common mode is within USB4 2.0 Specification limits

3.3.5.4 Test Method

1. The de-embedding of the cable assembly connecting TP2 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80GSa/s$ while keeping acquisition record length of 500 μs
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
3. Speed GEN4. Lane under test pattern PRTS7, remaining lanes shall be activated as aggressors transmitting PRTS19 with preset#0 to 50 Ω termination. SSC shall be enabled during the test
4. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50 Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
5. Capture the output common signal $(V_{TX-P} + V_{TX-N})/2$ while transmitting with best preset as reported in Transmitter Equalization test described in section 3.3.1 of current document (best preset is the one which produces lowest DDJ). The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
6. Run SigTest tool according to User Manual documentation (refer to section 6.2.5)
7. Check SigTest report for pass/fail status
8. Repeat the test for all remaining USB4 Transmitter Lanes

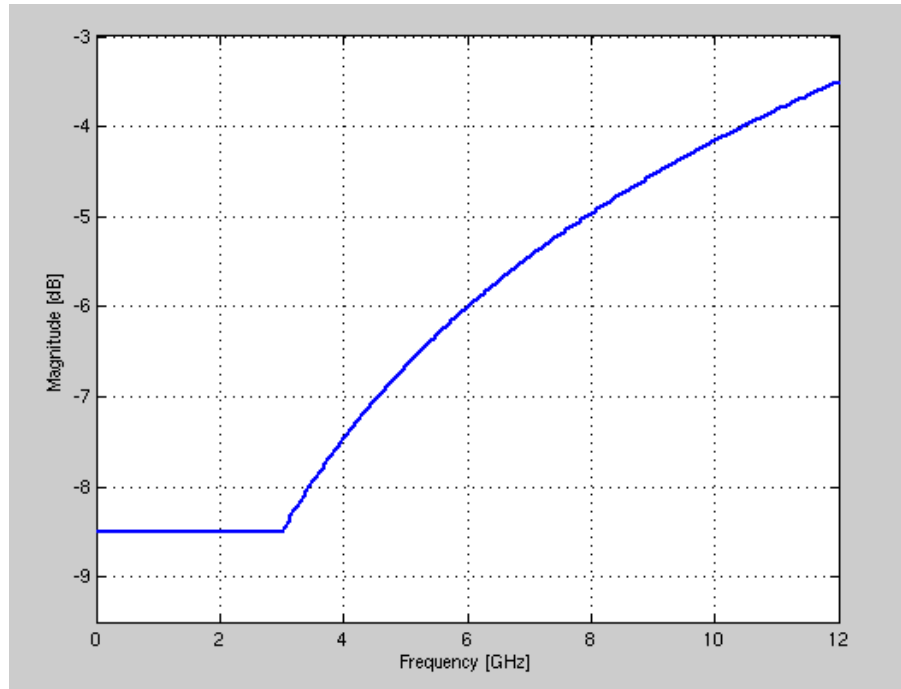
3.3.6 GEN4 Transmitter Return-Loss measurement (Informative)

3.3.6.1 Reference

RL_DIFF - USB4 Specification section 3.2.3.7

3.3.6.2 Requirement

$$SDD22(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 6 \\ -5.84 + 7.2 \cdot \log_{10}\left(\frac{f_{GHz}}{14}\right) & 6 < f_{GHz} \leq 14 \end{cases}$$



3.3.6.3 Test Objective

Confirm that the Transmitter Differential Return-Loss is within USB4 2.0 Specification limits

3.3.6.4 Test Method

1. Speed GEN4. Lane under test pattern PRTS7, remaining lanes shall be activated as aggressors transmitting PRTS19 with preset#0 to 50Ω termination. SSC shall be enabled during the test
2. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
3. Follow Appendix B for the Network Analyzer configuration
4. Calibrate the network analyzer and test cables using the manufacturers recommended 2-port calibration kit.
5. Connect Lane under test TX_P, TX_N at TP2 to the Network Analyzer.

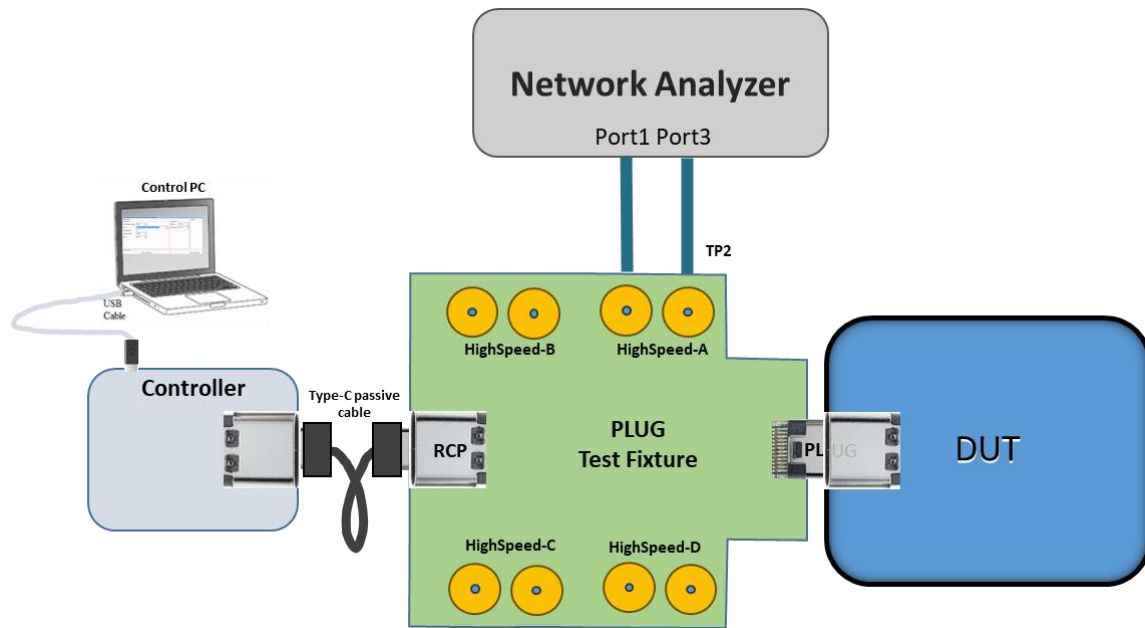


Figure 4. Transmitter Return Loss Test Setup

6. Capture the output s-parameter in s2p format while transmitting with best preset as reported in Transmitter Equalization test described in section 3.3.1 of current document (best preset is the one which produces lowest DDJ).
7. Run SigTest tool according to User Manual documentation (refer to section 6.2.6)
8. Check SigTest report for pass/fail status
9. Repeat the test for all remaining USB4 Transmitter Lanes

Note: The measurement shall be done at TP2 (including test fixture)

3.3.7 GEN4 Transmitter Integrated Return Loss

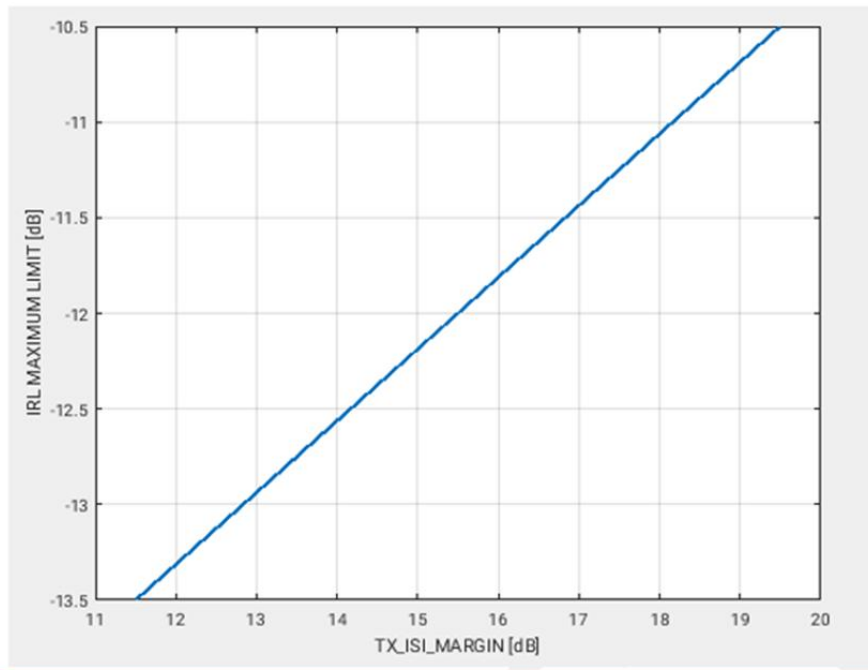
3.3.7.1 Reference

IRL - USB4 Specification section 3.2.3.6

3.3.7.2 Requirement

$$\text{IRL} \leq -13.5 + (\text{TX_ISI_MARGIN} - 11) \times 0.375$$

Figure 3-30. IRL Maximum Limit as a Function of TX_ISI_MARGIN



3.3.7.3 Test Objective

Confirm that the Transmitter Integrated Return-Loss is within USB4 2.0 Specification limits

3.3.7.4 Test Method

1. Run SigTest tool according to User Manual documentation (refer to section 6.2.6) using the corresponding s2p file captured in Transmitter Differential Return-Loss test and the corresponding waveform file used in Timing and Voltage measurement test (for TX_ISI_MARGIN)
2. Check SigTest report for pass/fail status
3. Repeat the test for all remaining USB4 Transmitter Lanes

3.3.8 GEN4 Transmitter LFPS

3.3.8.1 Reference

USB4 Specification Section 3.4, Table 3-33

Subset type	Symbol	Min	Max	Units
Timing Parameters subset	tPeriod	20	80	ns
	tPreData	80	120	ns
	tRiseFall		4	ns
	LFPS_DUTY_CYCLE	45	55	%
Voltage Parameters subset	V_CM_AC_LFPS		100	mV p-p
	V_TX_DIFF_PP_LFPS	800	1200	mV p-p

3.3.8.2 Test Objective

Confirm that the low frequency periodic signal transmitter all listed above timing and voltage parameters are within USB4 2.0 Specification limits

Confirm that the voltage level of Electrical Idle signal during tPreData is within USB4 2.0 Specification limits as described in section 3.3.4 of this document

Confirm that the following transitions are glitch-free: Electrical Idle to LFPS, LFPS to Electrical Idle, Electrical Idle to High-Speed

3.3.8.3 Test Method

1. Transmitter under test shall be configured to transmit the following sequence:
LFPS → Electrical Idle → High Speed PRBS11 as defined in USB4 2.0 specification Section 8.3.2.2.8, table 8-76, mode 001b, Speed GEN4
2. Transmitter under test shall be activated with maximum number of aggressor lanes configured as transmitters transmitting high speed PRTS19 with preset#0 to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test according to Appendix A.1.2 and aggressors according to Appendix A.2.3)
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of 10μs
 - No CDR, no average and no interpolation shall be used
4. The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range). LFPS shall be preceded by Electrical Idle for correct SigTest analysis
5. Run SigTest tool according to User Manual documentation (refer to section 14.1)
6. Repeat the test for all remaining USB4 Transmitter Lanes

4 Router Assembly Receiver Testing

This section describes the mandatory tests required for USB4 GEN4 Receiver compliance verification

The following sections provide detailed information on the setup and testing procedures of the USB4 GEN4 Receiver parameters. In the event of a discrepancy, the USB4 2.0 Specification prevails.

- Calibration shall be applied in cases where direct measurement is not feasible.
- USB4 v2 SigTest shall be used for all GEN4 Receiver testing and stress signal calibration (except TER testing)

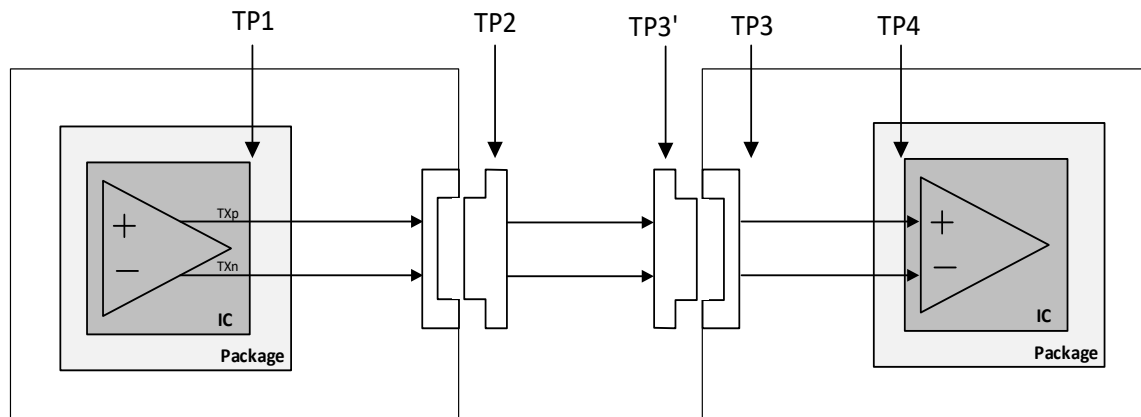


Figure 5. USB4 RX Compliance Points Definition

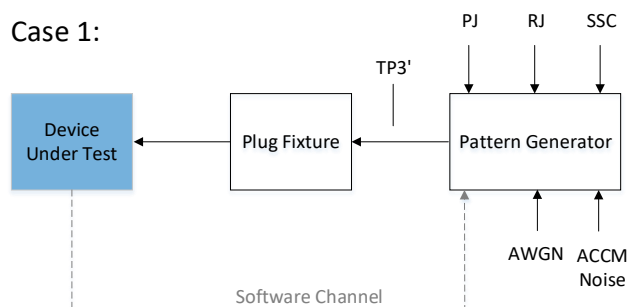
A Gen 4 receiver shall operate at a Trit Error Ratio (TER) of $1E-8$ or lower without Forward Error Correction when a stressed signal is driven at its input. Tolerance testing shall be performed while all neighboring transceivers are active. There are three test setups that shall be used for evaluating the Router Assembly receiver tolerance:

“Case1”, which addresses installations with low Insertion-Loss

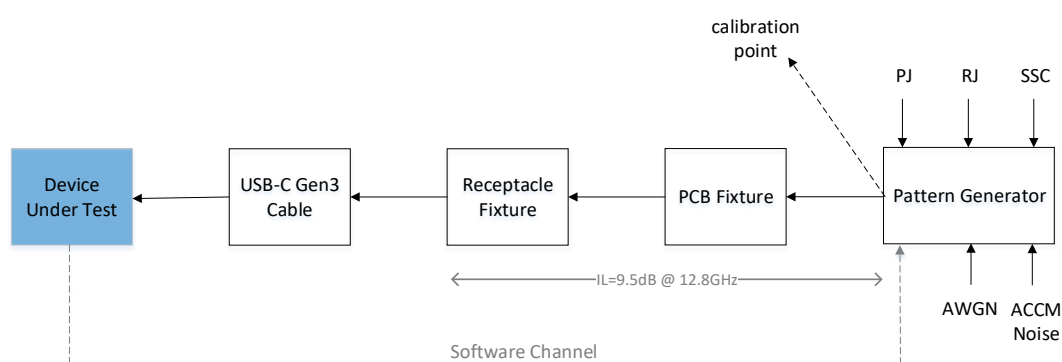
“Case2a”, which addresses passive cable installations with maximum Insertion - Loss. As part of this setup, the receiver under test shall be connected through a worst-case USB4 Gen 3 passive cable

“Case2b”, which addresses installations employing linear re-driver (LRD) cables. As part of this setup, the receiver under test shall be connected through a worst-case USB Type-C LRD cable

Case 1:



Case 2a:



Case 2b:

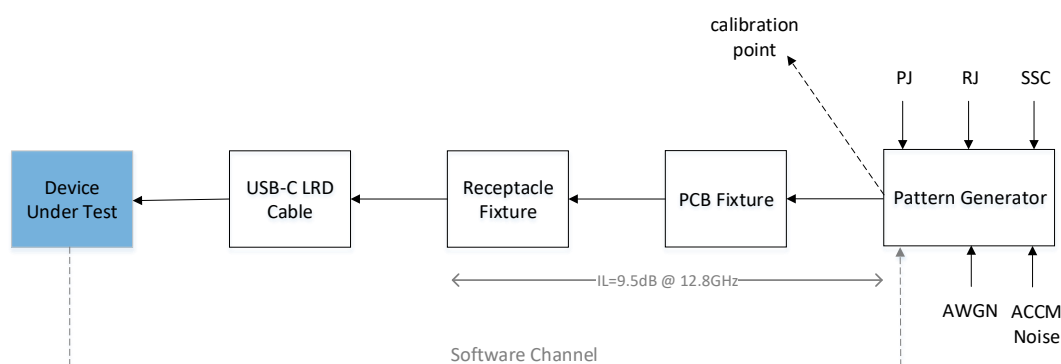


Figure 6. USB4 RX Tolerance Test Topologies

4.1 Receiver stress signal calibration

This section describes two calibration setups

1. BERT calibration to “worst case transmitter” for:
 - a. Case 1
 - b. Case 2a/2b at BERT output
2. Overall channel calibration to worst case condition

Note: Before beginning any test or data acquisition, the Generator and Scope must be warmed, calibrated, and cables de-skewed.

4.1.1 Calibration setup and BERT common settings

4.1.1.1 Calibration setup

The USB4 2.0 Specification outlines requirements for BERT output calibrations for case 1 and case 2 as measured at the USB Type-C connector at the plug side.

Connect the calibration setup as depicted in Figure 7 below.

- Connect DC blocks at BERT data out
- Connect pair of phase matched cables from the DC blocks to the oscilloscope
- No de-embedding of phase matched cables is required

4.1.1.2 BERT common settings

BERT common settings:

- GEN4 baud rate: 25.6GB
- Test pattern: PRTS7 (PAM3)
- TX FFE preset: preset #0 (Note: Constant preset #0 setting is applicable only during calibration process. During regular TER testing DUT Receiver is allowed to request any preset defined in the spec)
- SSC:
 - SSC rate: 32kHz
 - SSC downspread deviation:
 - Case1 0ppm to -3400ppm
 - Case2 0ppm to -3000ppm
 - SSC modulation shape: triangular
- Refer to section 4.1.4.1.3.3 to confirm BERT Insertion Loss (BERT_IL) before proceeding to the subsequent calibration steps

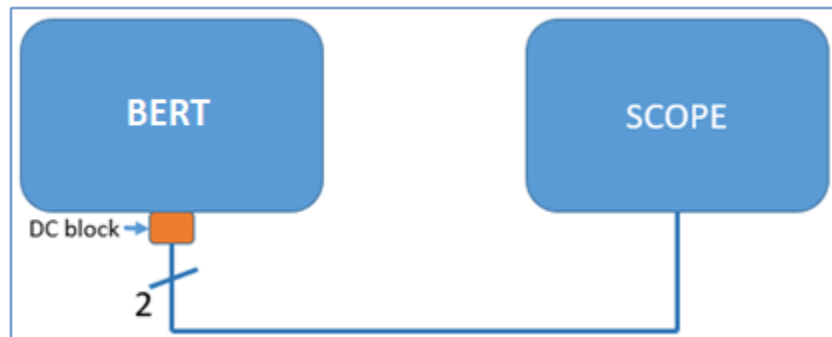


Figure 7. Receiver Calibration Setup – BERT output

4.1.2 BERT output calibration for case 1

1. Construct setup as described in section 4.1.1.1 of this document
2. Configure BERT as described in section 4.1.1.2 of this document

4.1.2.1 Voltage Swing

4.1.2.1.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.1.2 Requirement

Voltage Swing – 1090mV p-p \pm 15mV

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.1.3 Test Method

1. Turn all other impairments off
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
3. Capture single ended pair of the output signal
4. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
5. Check SigTest report for Voltage Swing result
6. Adjust BERT voltage swing setting and repeat steps 4-6 until desired result is achieved

Note:

1. Record the Oscilloscope vertical scaling setting (voltage/div) of the calibrated signal
2. See Appendix D of this document on scope intrinsic noise measurement for Receiver calibration procedure
3. Refer to User Manual documentation (refer to section 8.2) on scope intrinsic noise waveform usage. Scope intrinsic noise waveform shall be used for subsequent calibration steps
4. Once the Voltage Swing has been adjusted, the oscilloscope vertical scale setting shall remain constant for subsequent calibration steps

4.1.2.2 Level Mismatch

4.1.2.2.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.2.2 Requirement

Level Mismatch – 0.975 ± 0.005

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.2.3 Test Method

1. Keep Voltage Swing as calibrated in previous step
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for Level Mismatch result
7. Adjust BERT PAM3 level ratio setting and repeat steps 5-7 until desired result is achieved

4.1.2.3 RJ

4.1.2.3.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.3.2 Requirement

RJ – 0.0085UI rms \pm 0.0005UI

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.3.3 Test Method

1. Keep Voltage Swing, Level Mismatch as calibrated in previous steps
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for RJ result
7. Adjust BERT RJ amplitude setting and repeat steps 5-7 until desired result is achieved

4.1.2.4 SNDR

4.1.2.4.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.4.2 Requirement

SNDR – 34dB \pm 0.15dB

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.4.3 Test Method

1. Configure differential mode sinusoidal interference frequency setting to 10GHz
2. Keep Voltage Swing, Level Mismatch, RJ as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for SNDR result
8. Adjust BERT differential mode sinusoidal interference amplitude setting and repeat steps 5-7 until desired result is achieved

Note:

Adding differential sinusoidal interference might impact on the calibrated RJ value (as calibrated in section 4.1.2.3). The added RJ is not part of the RJ calibration, thus SigTest reported RJ parameter shall be ignored from this point on

Concurrent execution of steps 4.1.2.4 and 4.1.2.5 is permissible, although strongly unrecommended

4.1.2.5 ACCM

4.1.2.5.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.5.2 Requirement

ACCM – 100mV p-p \pm 10mV

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.5.3 Test Method

1. Configure common mode sinusoidal interference frequency setting to 400MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for ACCM result
8. Adjust BERT PAM3 common mode sinusoidal interference amplitude setting and repeat steps 6-8 until desired result is achieved

4.1.2.6 PJ

4.1.2.6.1 Reference

USB4 2.0 Specification Table 3-27

4.1.2.6.2 Requirement

PJ – 0.085UI p-p \pm 0.002UI

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.2.6.3 Test Method

1. Configure PJ frequency to 1MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR, ACCM as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for PJ result
8. Adjust BERT PJ amplitude setting and repeat steps 6-8 until desired result is achieved
9. Repeat for remaining PJ frequencies as defined in USB4 2.0 base spec (remaining PJ frequencies 2MHz, 10MHz, 50MHz, 100MHz)
10. Save BERT setup as **Test Case 1** per PJ frequency

4.1.3 BERT output calibration for case 2

1. Construct setup as described in section 4.1.1.1 of this document
2. Configure BERT as described in section 4.1.1.2 of this document

4.1.3.1 Voltage Swing

4.1.3.1.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.1.2 Requirement

Voltage Swing – 820mV p-p \pm 15mV

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.1.3 Test Method

1. Turn all other impairments off
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
3. Capture single ended pair of the output signal
4. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
5. Check SigTest report for Voltage Swing result
6. Adjust BERT voltage swing setting and repeat steps 4-6 until desired result is achieved

Note:

1. Record the Oscilloscope vertical scaling setting (voltage/div) of the calibrated signal
2. See Appendix D of this document on scope intrinsic noise measurement Receiver calibration procedure
3. Refer to User Manual documentation (refer to section 8.2) on scope intrinsic noise waveform usage. Scope intrinsic noise waveform shall be used for subsequent calibration steps
4. Once the Voltage Swing has been adjusted, the oscilloscope vertical scale setting shall remain constant for subsequent calibration steps

4.1.3.2 Level Mismatch

4.1.3.2.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.2.2 Requirement

Level Mismatch – 0.975 ± 0.005

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.2.3 Test Method

1. Keep Voltage Swing as calibrated in previous step
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for Level Mismatch result
7. Adjust BERT PAM3 level ratio setting and repeat steps 5-7 until desired result is achieved

4.1.3.3 RJ

4.1.3.3.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.3.2 Requirement

RJ – 0.0085UI rms \pm 0.0005UI

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.3.3 Test Method

1. Keep Voltage Swing, Level Mismatch as calibrated in previous steps
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for RJ result
7. Adjust BERT RJ amplitude setting and repeat steps 5-7 until desired result is achieved

4.1.3.4 SNDR

4.1.3.4.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.4.2 Requirement

SNDR – 34dB \pm 0.15dB

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.4.3 Test Method

1. Configure differential mode sinusoidal interference frequency setting to 10GHz
2. Keep Voltage Swing, Level Mismatch, RJ as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for SNDR result
8. Adjust BERT differential mode sinusoidal interference amplitude setting and repeat steps 5-7 until desired result is achieved

Note:

Adding differential sinusoidal interference might impact on the calibrated RJ value (as calibrated in section 4.1.2.3). The added RJ is not part of the RJ calibration, thus SigTest reported RJ parameter shall be ignored from this point on

Concurrent execution of steps 4.1.3.4 and 4.1.3.5 is permissible, although strongly unrecommended

4.1.3.5 ACCM

4.1.3.5.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.5.2 Requirement

ACCM – 100mV p-p \pm 10mV

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.5.3 Test Method

1. Configure common mode sinusoidal interference frequency setting to 400MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for ACCM result
8. Adjust BERT common mode sinusoidal interference amplitude setting and repeat steps 6-8 until desired result is achieved

4.1.3.6 PJ

4.1.3.6.1 Reference

USB4 2.0 Specification Table 3-27

4.1.3.6.2 Requirement

PJ – 0.075UI p-p \pm 0.002UI

Test Case	Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
1	1090	34	0.975	100	0.085	0.0085
2a+2b	820	34	0.975	100	0.075	0.0085

4.1.3.6.3 Test Method

1. Configure PJ frequency to 1MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR, ACCM as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for PJ result
8. Adjust BERT PJ amplitude setting and repeat steps 6-8 until desired result is achieved
9. Repeat for remaining PJ frequencies as defined in USB4 2.0 base spec (remaining PJ frequencies 2MHz, 10MHz, 50MHz, 100MHz)
10. Save BERT setup as **Test Case 2** per PJ frequency

4.1.4 Channel calibration to worst case condition

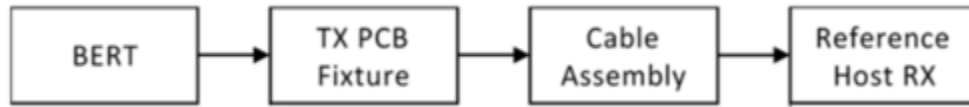


Figure 8. End-to-End channel for operating margin evaluation

Channel calibration to the worst case condition consists of three consequential stages:

1. BERT model extraction
2. Test Channel measurement
3. Link operating margin evaluation

4.1.4.1 BERT model extraction

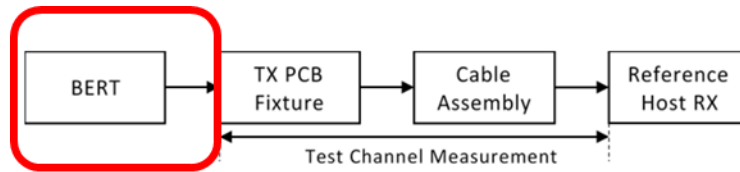
4.1.4.1.1 Reference

USB4 Specification section 3.2.4.2, case 2 related paragraph

4.1.4.1.2 Requirement

Extract BERT assembly model by measuring:

1. Differential Return-Loss measured at BERT assembly output
2. Differential Insertion-Loss of the BERT assembly extracted by measuring step response at its output for deriving the corresponding impulse response and transforming to the frequency domain



4.1.4.1.3 Test Method

4.1.4.1.3.1 Differential Return-Loss measurement at BERT assembly output

1. Follow Appendix B for the Network Analyzer configuration
2. Calibrate the Network Analyzer and test cables using a 2-port auto calibration kit
3. Construct a Test setup as shown in Figure 9. The coax phase matched cables shall be used in TER test setup as shown in section 4.2.3, Figure 13
4. Configure BERT to transmit PAM2 SQ256 (128 Level2 and 128 Level0) with Swing of 820mV p-p and preset0
5. Turn all impairments off (Impairments are: RJ, PJ, Common and Differential Interferences, Level Mismatch, SSC)
6. Capture the output s-parameters
7. Save the s-parameter file in s2p format as **BERT_Sdd22.s2p** (it will be used later in *Link operating margin evaluation stages*)

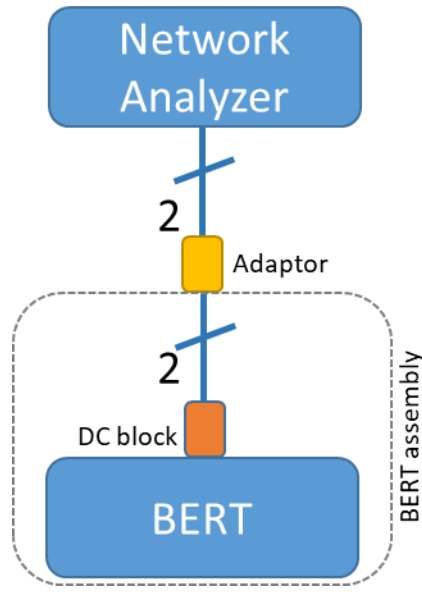


Figure 9. Test setup for BERT assembly Return-Loss extraction

4.1.4.1.3.2 BERT assembly step response extraction

1. Construct a Test setup as shown in figure 10. The coax phase matched cables shall be used in TER test setup as shown in section 4.2.3, Figure 13
2. Configure BERT to transmit PAM2 SQ256 (128 Level2 and 128 Level0) with Swing of 820mV p-p and preset0
3. Turn all impairments off (Impairments are: RJ, PJ, Common and Differential Interferences, Level Mismatch, SSC)
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $50\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
5. Capture the differential output signal
6. Save the waveform file as **BERT_Sdd21.[scope format]** (it will be used later in *Differential Insertion-Loss of the BERT assembly extraction* and *Link operating margin evaluation* stages)

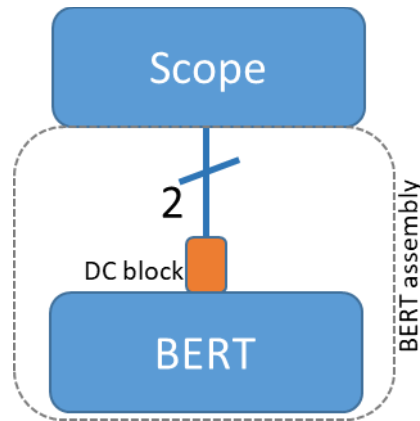


Figure 10. Test setup for BERT assembly step response extraction

4.1.4.1.3.3 Differential Insertion-Loss of the BERT assembly extraction

1. Run SigTest tool according to User Manual documentation (refer to section 8.3.2)

- Input file is:
 - BERT_Sdd21.[scope format]
- Output parameters are:

BERT Insertion Loss (IL)
BERT_IL _{12.8GHz}
BERT_IL _{3.2GHz} - BERT_IL _{6.4GHz}
BERT_IL _{6.4GHz} - BERT_IL _{12.8GHz}

2. Verify that the BERT assembly Insertion-Loss parameters are within specification limits defined in section 2.2.3 of this document (BERT_IL is negative value). If it passes, proceed to 3. Otherwise, contact the BERT vendor support group for further assistance
3. Use BERT assembly Insertion-Loss @ 12.8GHz in Test channel measurement section (BERT_IL is negative value)

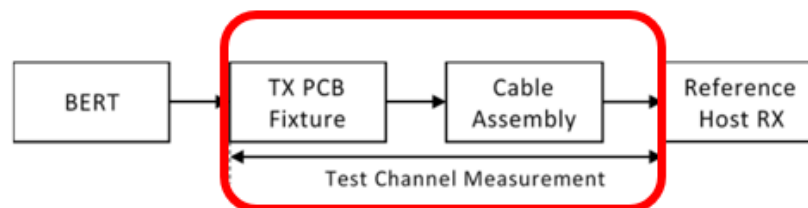
4.1.4.2 Test channel measurement

4.1.4.2.1 Reference

USB4 Specification section 3.2.4.2, case 2 related paragraph

4.1.4.2.2 Requirement

Measure the s-parameters of the Test channel defined by TX PCB fixture and cable assembly



USB Type-C passive cable assembly Insertion Loss Fit (ILfit) target shall be -7.5 @ 10GHz and -9.5dB @ 12.8GHz with tolerance range of [-0 : + 1] and [-0 : + 1.5]dB respectively per every physical lane pair being used for receiver testing

Note: USB Type-C GEN3 passive cable assembly shall meet the requirements specified by the most current version of Chapter 3 of the USB Type-C Cable and Connector Specification and USB Type-C Connectors and Cable Assemblies Compliance Document

Test Channel with Receptacle fixture de-embedded recommended insertion loss target should be (-19dB – BERT_IL) @ 12.8GHz \pm 0.5dB

The mandatory End to End channel Ifit target requirement is described in section 4.1.4.3, Link operation margin evaluation

In case receiver asymmetric mode is supported by DUT, the asymmetric receiver lanes shall be tested using another passive cable physical lane pair. Thus the test channel calibration and following link operating margin evaluation shall be done per every passive cable physical lane pair being used, calibration for symmetric lanes and additional calibration for asymmetric lanes

4.1.4.2.3 Test Method

1. Follow Appendix B for the Network Analyzer configuration
2. Construct a Test Channel setup as shown in Figure 11
3. Capture Test Channel s-parameters in s4p format
4. Remove Receptacle fixture trace loss from Test Channel s-parameters by analytical means. The USB Type-C cable and connector specification methodology shall be used for receptacle test fixture trace loss de-embedding by using 2xThru structure. Verify the accuracy of the analytical tool's de-embedding process by conducting a comparison check between the cascaded de-embedded components and the original one s-parameter measurement
5. Record Test Channel with Receptacle fixture de-embedded Insertion Loss at 12.8GHz
6. If Insertion Loss target is not achieved
 - Adjust PCB fixture Insertion Loss
 - Repeat step 3-6
7. If Insertion Loss target is achieved
 - Save Test Channel with Receptacle fixture trace de-embedded s-parameters file in s4p format as **Test_Channel.s4p** (it will be used later in link operating margin evaluation stage)

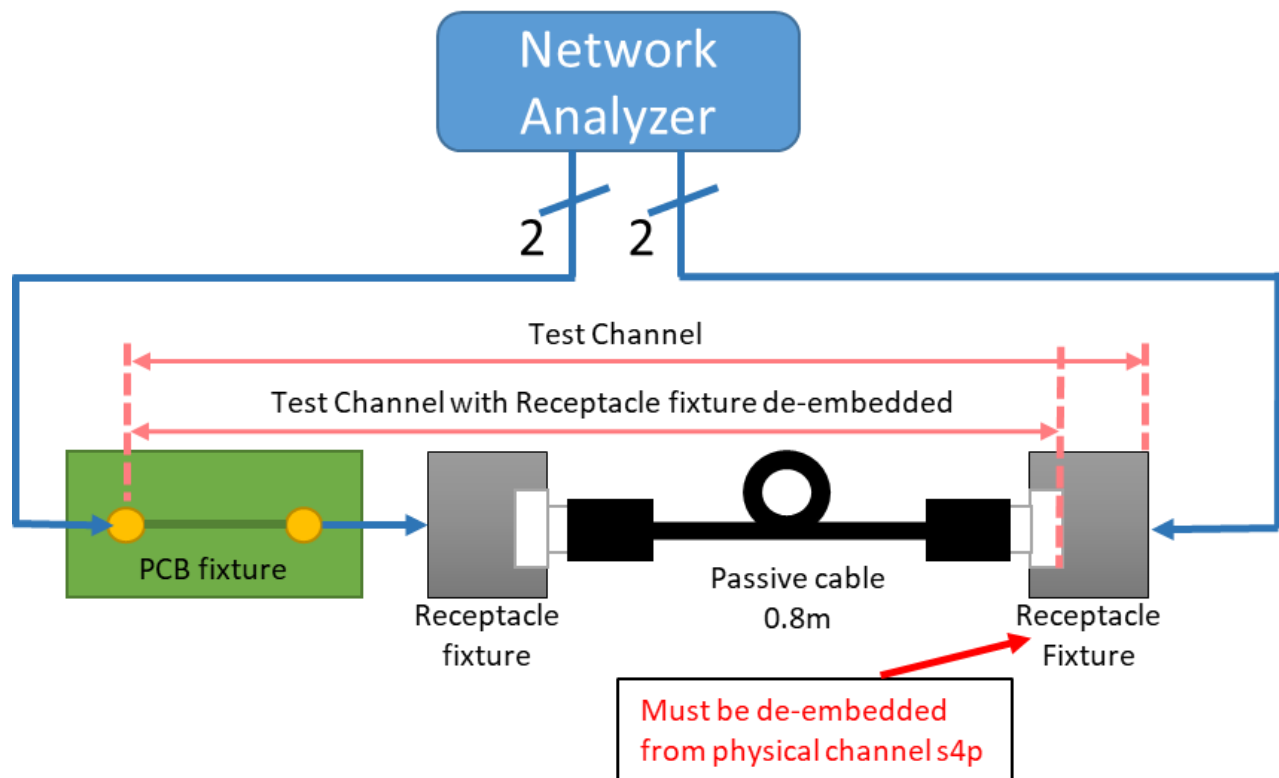


Figure 11. Test Channel setup

4.1.4.3 Link operating margin evaluation

4.1.4.3.1 Reference

USB4 Specification section 3.2.4.2, case 2 related paragraph

4.1.4.3.2 Requirement

Evaluate the Link operating margin over the cascaded end-to-end channel using SigTest tool for calibrating the correct setup operating conditions. It is required to complete Test Channel measurements and BERT assembly model extraction prior to proceeding to this section.

The end-to-end channel Insertion Loss Fit (ILfit) target at Nyquist is defined as $-29\text{dB} \pm 0.5\text{dB}$ @ 12.8GHz, verified by SigTest tool using the ILfit function as defined in USB Type-C cable and connector specification (section 3.7.2.5). In case the extracted end-to-end channel ILfit at Nyquist is out of defined 1dB tolerance window, SigTest tool aborts with notification requesting Test Channel adjustments.

Following the operating margin evaluation, SigTest tool defines the required setup adjustments for aligning the setup to the end-to-end operating margin target, ECOM convergence value $0\text{dB} \pm 0.1\text{dB}$, through BERT SJ magnitude adjustments with limited maximum range of 10mUI. In case the end-to-end operating margin is far-off the target, SigTest tool aborts with notification requesting Test Channel adjustments

4.1.4.3.3 Test Method

1. Run SigTest tool according to User Manual documentation (refer to section 8.3.3)
 - Input files are:
 - Test_Channel.s4p
 - BERT_Sdd22.s2p
 - BERT_Sdd21.[scope format]
 - Output parameters are:
 - The extracted end-to-end channel ILfit at Nyquist
 - The amount of BERT SJ magnitude which shall be adjusted (the amount is relative number for addition/reduction, the amount is after applying reference CDR mask). Single value for all SJ frequencies
 - ECOM convergence values
2. Complete required adjustments:
 - Recall BERT calibration setup for **Test Case 2**
 - Adjust SJ magnitude for every SJ frequency (refer to section 4.1.3.6 of this document for test procedure)
4. Save BERT setup as **Test Case 2** per SJ frequency

4.2 GEN4 Receiver TER Test Procedure

Following section describes the GEN4 Receiver test procedure for Case 1 and Case 2a/b. GEN4 receiver shall operate at a Trit Error Ratio (TER) of $1E-8$ or lower without Forward Error Correction when a stressed signal is driven at its input.

Error counter check shall be completed once per lane (case 1 or case 2) at single PJ frequency

It is the user's responsibility to confirm the accuracy of the BERT TXFFE coefficients with the BERT vendor, ensuring they fall within the tolerance ranges specified in section 2.2.3 of this document

4.2.1 GEN4 Receiver equalization training for TER test

4.2.1.1 Reference

USB4 Specification section 3.2.4.2, equalization training paragraph

4.2.1.2 Requirement

Following section describes GEN4 Receiver equalization training sequence which applies for both compliance test cases: case 1 and case 2a/b

4.2.1.3 Test Method

1. Configure BERT to transmit PRBS11 PAM2 at GEN4 nominal baud rate with stressed signal calibration setup for case 1 or case2a/b without applying SSC down-spreading
2. BERT shall send ACK message once completed
3. Receiver under test shall complete equalization training #1 with PRBS11. During equalization process FFE handshake is activated
4. Receiver shall present "PAM3 without SSC ready" indication once equalization training #1 is completed
5. BERT shall switch pattern to PRTS7 PAM3 at GEN4 baud rate without applying SSC down-spreading. The switching from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document
6. BERT shall send pattern switch request ACK message once completed
7. Receiver under test shall complete equalization training #2 with PRTS7. During equalization process FFE handshake is activated
8. Receiver shall present "PAM3 with SSC ready" indication once equalization training #2 is completed
9. BERT shall switch pattern to PRTS19 PAM3 at GEN4 baud rate with Pre-Coding enabled, applying SSC down-spreading of 0ppm to -3400ppm for case 1 and SSC down-spreading of 0ppm to -3000ppm for case 2a/b. The switching from PRTS7 to PRTS19 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document. The SSC activation shall be done in a glitch-free manner such that the SSC modulation profile starts from the BERT's initial frequency as defined in section 2.2.3 of this document. SSC down-spreading and Pre-Coding enablement allowed to be asynchronous within 500usec from pattern change
10. BERT shall send pattern switch request ACK message once completed
11. Proceed to TER testing

Note: Equalization training process is part of Receiver testing and managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.2.2 GEN4 TER test case 1

4.2.2.1 Reference

USB4 Specification section 3.2.4.2

4.2.2.2 Test setup

Construct setup as shown in Figure 12. Use passive cable without Emark to connect USB4 micro-controller to the DUT as shown below. USB4 Micro-controller is connected to Control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT)

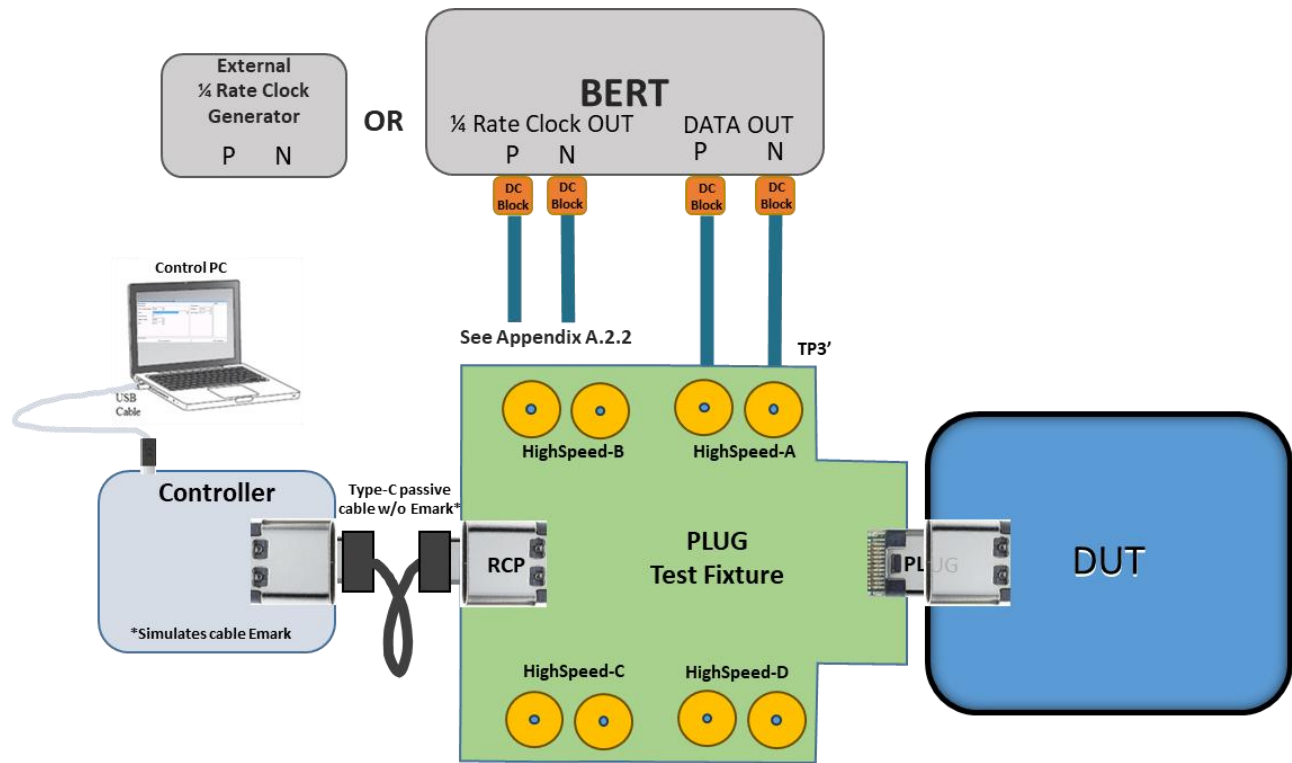


Figure 12. Receiver Test Setup for case 1

4.2.2.3 Test Method

1. Recall Test Case 1 calibrated setup that was saved in Section 4.1.2.6 of this document
3. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
4. Initiate Equalization training flow as described in Section 4.2.1 of this document
5. Error counter check phase (skip this section if done already for this Lane):

- Initiate continuous random symbol error stream injection targeting TER ratio of $1\text{E-}6$ using BERT
- Start TER test
- Wait 3sec
- End TER test
- Read TER ratio as reported by ETT
- If TER ratio result is $1\text{E-}6 \pm 1.5\text{E-}7$ then Pass, else Fail
- Error injection with reduced/disabled jitter impairments is acceptable
- Error counter check shall be performed once per lane

6. TER test phase:

- In case jitter impairments were changed during error counter check phase, repeat equalization training (steps 1-3)
- Start TER test
- Wait 30sec
- End TER test
- Read TER ratio as reported by ETT
- If TER ratio $< 1\text{E-}8$ then Pass, else Fail

7. Repeat all steps above including equalization training for each PJ frequency: 1MHz, 2MHz, 10MHz, 50MHz and 100MHz

8. Repeat all steps above for each Receiver Lane

Note: Receiver testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.2.3 GEN4 TER test case 2

4.2.3.1 Reference

USB4 Specification section 3.2.4.2

4.2.3.2 Test setup

Construct setup as shown in Figure 13. Connect USB4 micro-controller directly to Type-C plug connector of the test fixture as shown below. USB4 Micro-controller is connected to control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT). Use BERT assembly and Test Channel as calibrated in sections 4.1.4.1 and 4.1.4.2 respectively of this document

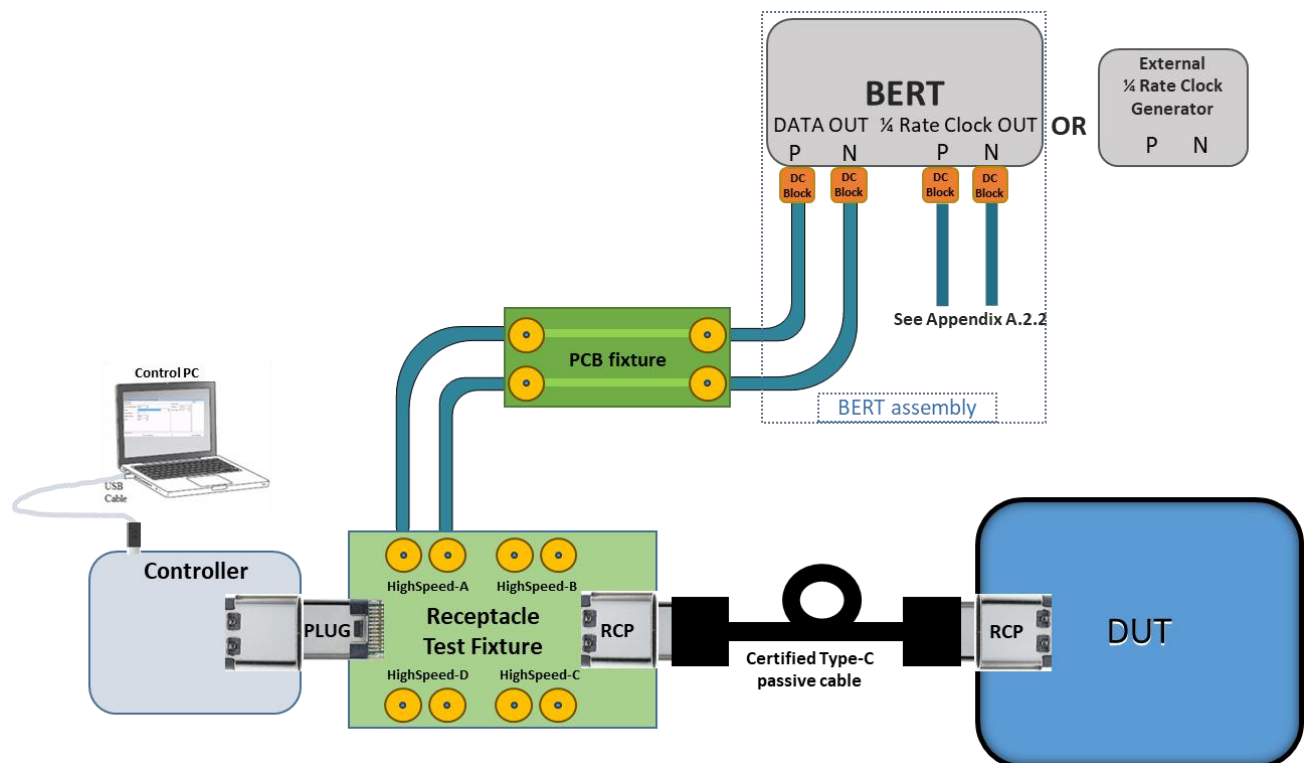


Figure 13. Receiver Test Setup for case 2

4.2.3.3 Test Method

1. Recall Test Case 2 calibrated setup that was saved in Section 6.1.3.6 of this document
2. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
3. Initiate Equalization training flow as described in Section 4.2.1 of this document
4. Error counter check phase (skip this section if done already for this Lane):

- Initiate continuous random symbol error stream injection targeting TER ratio of 1E-6 using BERT
 - Start TER test
 - Wait 3sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio result is $1E-6 \pm 1.5E-7$ then Pass, else Fail
 - Error injection with reduced/disabled jitter impairments is acceptable
5. TER test phase:
 - In case jitter impairments were changed during error counter check phase, repeat equalization training (steps 1-3)
 - Start TER test
 - Wait 30sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio < 1E-8 then Pass, else Fail
 6. Repeat all steps above including equalization training for each PJ frequency: 1MHz, 2MHz, 10MHz, 50MHz and 100MHz
 7. Repeat all steps above for each Receiver Lane. In case of asymmetric lanes use proper calibrated physical channel
 8. Replace USB4 passive cable with USB4 LRD cable (The LRD cable shall be e-marked) and repeat steps 1-7

Note: Receiver testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.3 GEN4 Receiver Frequency Variation Training Test

4.3.1 Receiver Frequency Variation calibration for case 1

1. Construct the setup as shown in Figure 7 and following section 4.1.1
2. Recall Test Case 1 calibrated setup for PJ 100MHz, saved in Section 4.1.2.6 of this document
3. Configure BERT to output PRTS7 with SSC down-spreading disabled
4. Construct the frequency variation dynamics as shown in Figure 14a. Refer to USB4 2.0 Specification Table 3-26. Tolerance is $\pm 25\text{ppm}$ with respect to USB4 2.0 Specification targets

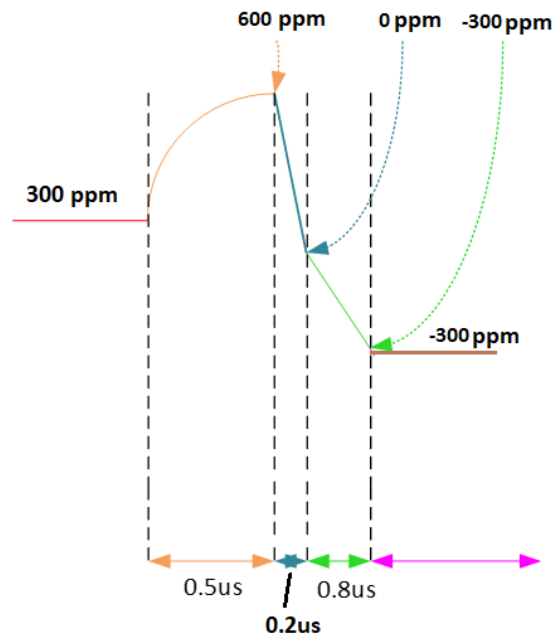


Figure 14a. Frequency variation dynamics

5. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
 - Set triggering capabilities to capture this event. Make sure to capture event entirely (initial frequency, clock switch and steady state after clock switch)
6. Capture the differential output signal with frequency variation dynamics
7. Run SigTest tool according to User Manual documentation (refer to section 8.4.1)
8. Check SigTest report for frequency variation parameters
9. Adjust frequency variation dynamics setting and repeat steps 6-8 until desired result is achieved
10. Save setup as **RX frequency variation Test Case 1**

4.3.2 Receiver Frequency Variation calibration for case 2

1. Construct the setup as shown in Figure 7 and following section 4.1.1
2. Recall Test Case 2 calibrated setup for PJ 100MHz, saved in Section 4.1.3.6 of this document
3. Configure BERT to output PRTS7 with SSC down-spreading disabled
4. Construct the frequency variation dynamics as shown in Figure 14b. Refer to USB4 2.0 Specification Table 3-26. Tolerance is ± 25 ppm with respect to USB4 2.0 Specification targets

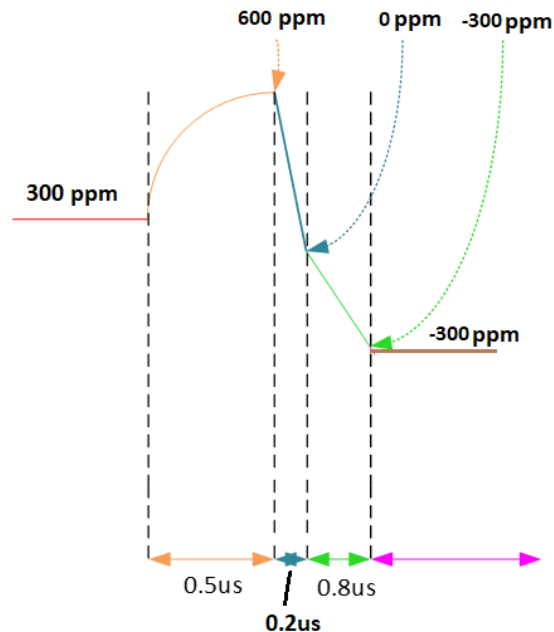


Figure 14b. Frequency variation dynamics

5. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate ≥ 80 GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
 - Set triggering capabilities to capture this event. Make sure to capture event entirely (initial frequency, clock switch and steady state after clock switch)
6. Capture the differential output signal with frequency variation dynamics
7. Run SigTest tool according to User Manual documentation (refer to section 8.4.1)
8. Check SigTest report for frequency variation parameters
9. Adjust frequency variation dynamics setting and repeat steps 6-8 until desired result is achieved

Save setup as **RX frequency variation Test Case 2**

4.3.3 Receiver equalization training for Frequency Variation test

4.3.3.1 Reference

USB4 Specification section 3.2.4.2

4.3.3.2 Requirement

Following section describes GEN4 Receiver equalization training sequence which applies for frequency variation test

4.3.3.3 Test Method

1. Configure BERT to transmit PRBS11 PAM2 at GEN4 baud rate with stressed signal calibration setup for case 1 or case2a/b without applying SSC down-spreading
2. BERT shall send ACK message once completed
3. Receiver under test shall complete equalization training #1 with PRBS11. During equalization process FFE handshake is activated
4. Receiver shall present "PAM3 without SSC ready" indication once equalization training #1 is completed
5. BERT shall switch pattern to PRTS7 PAM3 at GEN4 baud rate without applying SSC down-spreading. The switching from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document
6. BERT shall send pattern switch request ACK message once completed
7. Receiver under test shall complete equalization training #2 with PRTS7. During equalization process FFE handshake is activated
8. Receiver shall present "PAM3 with SSC ready" indication once equalization training #2 is completed
9. Proceed to Receiver Frequency Variation testing

Note: Receiver frequency variation testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.3.4 Receiver Frequency Variation test case 1

4.3.4.1 Reference

Refer to USB4 2.0 Specification Table 3-26

Refer to Appendix F of this document for test flow diagram

4.3.4.2 Requirement

TER ratio $\leq 1\text{E-}4$

4.3.4.3 Test Objective

Confirm that the Receiver don't lose lock and record errors when frequency variation is applied.

4.3.4.4 Test Method

1. Construct the setup as shown in Figure 12, Section 4.2.2 of this document
2. Recall **RX frequency variation Test Case 1** saved in Section 4.3.1 of this document
3. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50 Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
4. Initiate Receiver equalization training as described in Section 4.3.3 of this document
5. TER test phase:
 - If TS2.clksw pattern is not required for this test by DUT, follow TER test TYPE I or TYPE II
 - If TS2.clksw pattern is required for this test by DUT, follow TER test TYPE II only
- 5.1. TYPE I
 - Start TER test on PRTS7
 - Send clock switch request command to BERT. BERT shall apply clock switch dynamics as calibrated in Section 4.3.1 of this document. Update query status on success in less than 1sec, Else test status is Fail
 - Wait for 2sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio $< 1\text{E-}4$ then Pass, else Fail
- 5.2. TYPE II
 - Start TER test on PRTS7 (transmitted by BERT) and send Compliance Port Operation with Pattern set to PRTS7

- Switch to TS2.clksw pattern right after TER test start while continuing to promote PRTS7 bits in the background
- Wait 2μsec
- Apply clock switch event within next 8μsec. BERT shall apply clock switch dynamics as calibrated in Section 4.3.1 of this document
- Switch back to PRTS7 10μsec after switching to TS2.clksw at the exact bit position it would have been if there had been no switch to TS2.CLKSW but continuous PRTS7
- Wait for 2sec
- End TER test
- Read TER ratio as reported by ETT
- If TER ratio < 1E-4 then Pass, else Fail

6. Repeat steps 2-5 10 times

7. Repeat all steps above for each Receiver Lane

Note: Receiver frequency variation testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.3.5 Receiver Frequency Variation test case 2

4.3.5.1 Reference

Refer to USB4 2.0 Specification Table 3-26

Refer to Appendix F of this document for test flow diagram

4.3.5.2 Requirement

TER ratio $\leq 1\text{E-}4$

4.3.5.3 Test Objective

Confirm that the Receiver don't lose lock and record errors when frequency variation is applied.

4.3.5.4 Test Method

1. Construct the setup as shown in Figure 13, Section 4.2.3 of this document
2. Recall **RX frequency variation Test Case 2** saved in Section 4.3.2 of this document
3. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50 Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
4. Initiate Receiver equalization training as described in Section 4.3.3 of this document
5. TER test phase:
 - If TS2.clksw pattern is not required for this test by DUT, follow TER test TYPE I or TYPE II
 - If TS2.clksw pattern is required for this test by DUT, follow TER test TYPE II only
- 5.1. TYPE I
 - Start TER test on PRTS7
 - Send clock switch request command to BERT. BERT shall apply clock switch dynamics as calibrated in Section 4.3.2 of this document. Update query status on success in less than 1sec, Else test status is Fail
 - Wait for 2sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio $< 1\text{E-}4$ then Pass, else Fail
- 5.2. TYPE II
 - Start TER test on PRTS7 (transmitted by BERT) and send Compliance Port Operation with Pattern set to PRTS7

- Switch to TS2.clksw pattern right after TER test start while continuing to promote PRTS7 bits in the background
 - Wait 2μsec
 - Apply clock switch event within next 8μsec. BERT shall apply clock switch dynamics as calibrated in Section 4.3.2 of this document
 - Switch back to PRTS7 10μsec after switching to TS2.clksw at the exact bit position it would have been if there had been no switch to TS2.CLKSW but continuous PRTS7
 - Wait for 2sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio < 1E-4 then Pass, else Fail
6. Repeat steps 2-5 10 times
7. Repeat all steps above for each Receiver Lane. In case of asymmetric lanes use proper calibrated physical channel

Note: Receiver frequency variation testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

4.4 GEN4 Receiver Return-Loss (Informative)

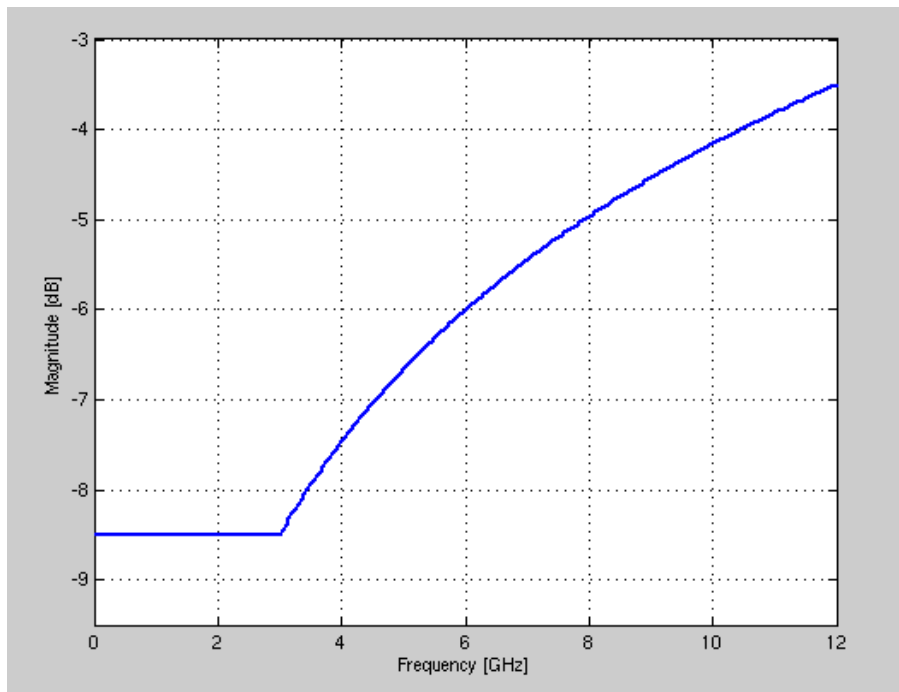
4.4.1 GEN4 Receiver Return-Loss measurement (Informative)

4.4.1.1 Reference

RL_DIFF - USB4 Specification section 3.2.4.1.2

4.4.1.2 Requirement

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < f_{GHz} \leq 6 \\ -5.84 + 7.2 \cdot \log_{10}\left(\frac{f_{GHz}}{14}\right) & 6 < f_{GHz} \leq 14 \end{cases}$$



4.4.1.3 Test Objective

Confirm that the Receiver Differential Return-Loss is within USB4 2.0 Specification limits

4.4.1.4 Test Method

1. Follow Appendix B for the Network Analyzer configuration
2. Calibrate Network Analyzer using a 2-port auto calibration kit
3. Construct setup as shown in Figure 15. Use passive cable without Emark to connect USB4 micro-controller to the DUT as shown below
4. Connect Lane under test RX_P, RX_N at TP2 to the Network Analyzer.

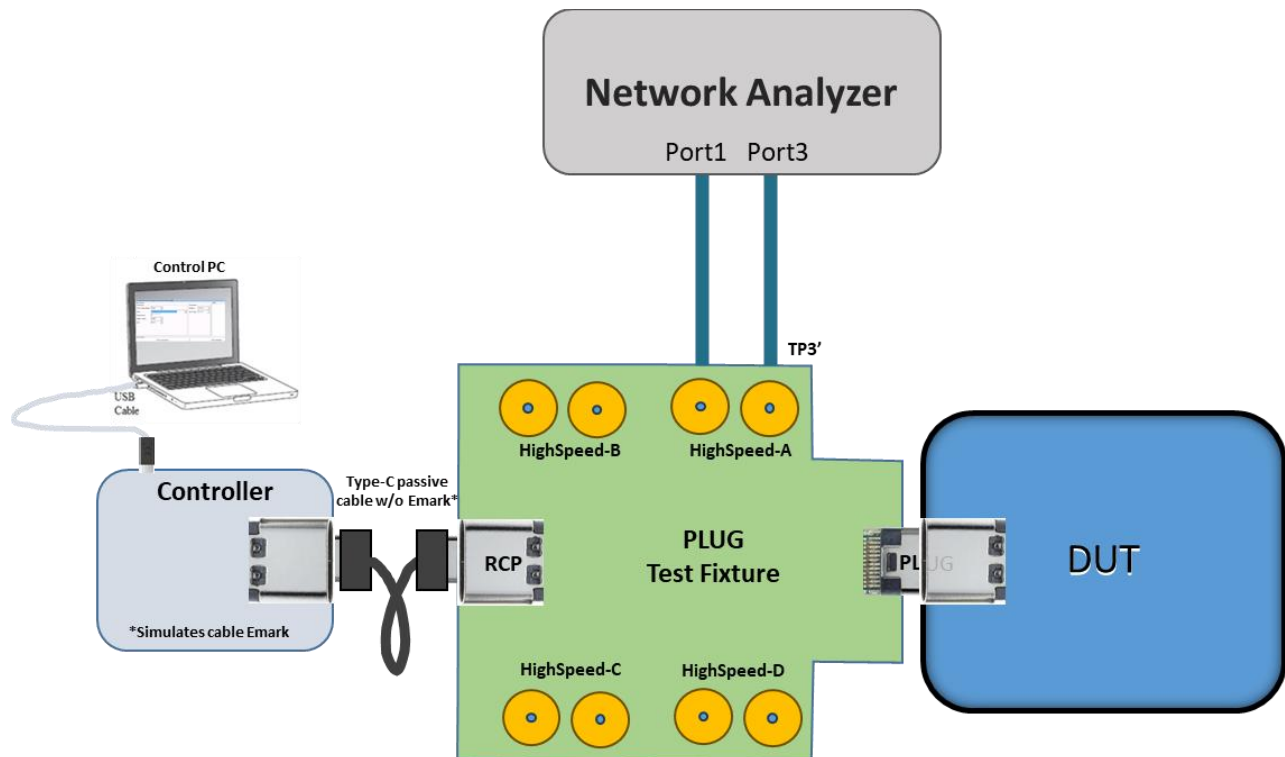


Figure 15. Receiver Return Loss Test Setup

5. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation). Quarter rate clock aggressors shall be not activated in this test
6. Capture s-parameter in s2p format
7. Run SigTest tool according to User Manual documentation (refer to section 8.4.2)
8. Check SigTest report for pass/fail status
9. Repeat the test for all remaining USB4 Receiver Lanes

Note: The measurement shall be done at TP2 (including test fixture)

4.4.2 GEN4 Receiver Integrated Return-Loss measurement (Informative)

4.4.2.1 Reference

IRL - USB4 2.0 Specification Table 3-26 and section 3.2.4.1.1 - Informative

4.4.2.2 Requirement

$IRL \leq -13.5\text{dB}$

4.4.2.3 Test Objective

Confirm that the Receiver Integrated Return Loss is within USB4 2.0 Specification limits

4.4.2.4 Test Method

1. Run SigTest tool according to User Manual documentation (refer to section 8.3.2) using the corresponding s2p file captured in Receiver Differential Return-Loss test
2. Check SigTest report for pass/fail status
3. Repeat the test for all remaining USB4 Receiver Lanes

4.5 GEN4 Receiver LFPS

4.5.1 Reference

USB4 Specification Section 3.4, Table 3-33

Symbol	Min	Max	Units
V_LFPS_RX_DETECT_TH	100	300	mV p-p

4.5.2 Test Objective

Confirm that the low frequency periodic signal receiver properly detects incoming LFPS signal with voltage swing at 300mV and above

Confirm that the low frequency periodic signal receiver doesn't detect incoming LFPS signal with voltage swing at 100mV and below

Confirm that the low frequency periodic signal receiver properly detects incoming LFPS signal with each of the following calibrated to the specification limit BERT LFPS signal:

- Voltage Swing Min/Max (V_TX_DIFF_PP_LFPS)
- Period Min/Max (tPeriod)
- Duty Cycle Min/Max (LFPS_DUTY_CYCLE)
- Common mode noise Max (V_CM_AC_LFPS)

Confirm that the described above detection scenarios are stable at least within time period of 5sec

4.5.3 Calibration

1. Construct the setup as described in section 4.1.1.1 of this document
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of 10 μs
 - No CDR, no average and no interpolation shall be used
3. The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range). LFPS shall be preceded by Electrical Idle for correct SigTest analysis
4. Capture LFPS single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 14.3)
6. Check SigTest report for parameter results according to setup #1 listed in table below
7. Adjust BERT settings and repeat steps 3-6 until desired parameters targets are achieved
8. Save BERT setup #1
9. Repeat steps 3-8 for each setup #2-9 listed in table below

Setup #	Swing	tPeriod	Duty Cycle	ACCM [mVpp]	Comments
---------	-------	---------	------------	-------------	----------

	[mV]	[ns]	[%]		
1	800	50	50	Off	Min swing
2	1200	50	50	Off	Max swing
3	1000	20	50	Off	Min tPeriod
4	1000	80	50	Off	Max tPeriod
5	1000	50	45	Off	Min duty cycle
6	1000	50	55	Off	Max duty cycle
7	300	50	50	Off	Above V_LFPS_RX_DETECT_TH max
8	100	50	50	Off	Below V_LFPS_RX_DETECT_TH min
9	1000	50	50	100	With ACCM

Calibration tolerance ranges:

Stress parameter	Target Value	Min	Max
Swing	800mV	800mV	810mV
Swing	1000mV	990mV	1010mV
Swing	1200mV	1190mV	1200mV
Swing	300mV	300mV	305mV
Swing	100mV	95mV	100mV
tPeriod	20ns	20ns	21ns
tPeriod	50ns	49.5ns	50.5ns
tPeriod	80ns	79ns	80ns
Duty cycle	45	45	45.5
Duty cycle	50	49.5	50.5
Duty cycle	55	54.5	55
ACCM	100mV	100mV	105mV

4.5.4 Test Setup

Construct setup as shown in Figure 16 below. Use passive cable without Emark to connect USB4 micro-controller to the DUT as shown below. USB4 Micro-controller is connected to Control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT)

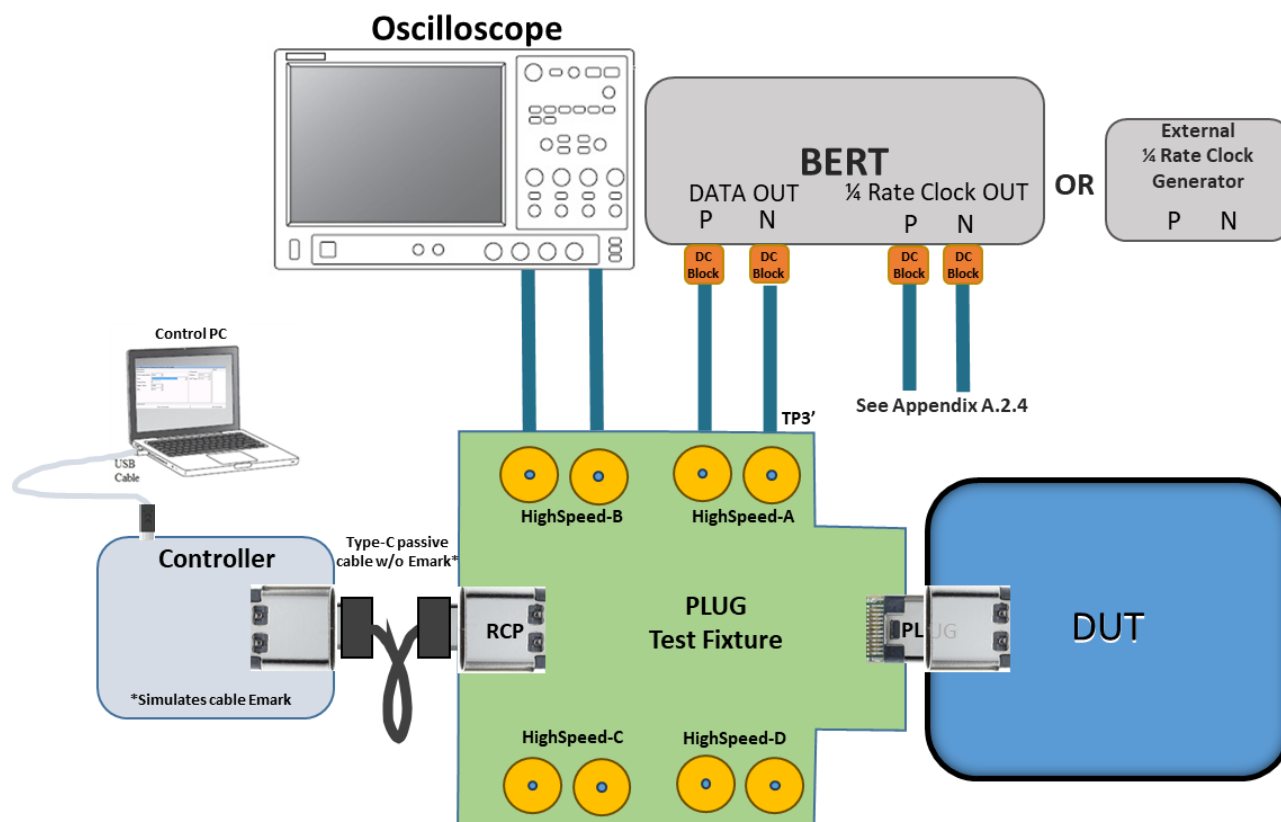


Figure 16. Receiver LFPS Test Setup

4.5.5 Test Method

1. Construct the setup as shown in Figure 16
2. Receiver under test shall be configured to detect the incoming LFPS signal as defined in USB4 2.0 specification Section 8.3.2.2.8, table 8-76, mode 011b, Speed GEN4. The detection observation shall be done through adjacent transmitter which shall transmit LFPS when it detects LFPS on receiver under test and shall move to electrical idle when not detecting LFPS on receiver under test
3. Receiver under test shall be activated with maximum number of aggressor lanes configured as transmitters transmitting high speed PRTS19 signal to 50Ω. Activate Receivers, incoming signal detection is not required (Configure Lane under test according to Appendix A.1.2 and aggressors according to Appendix A.2.4)
4. Recall calibrated setup saved in Section 4.5.3 of this document
5. Initiate LFPS Receiver test and observe LFPS Transmitter output for 5sec while triggering the scope on:
 - No signal or Electrical idle for setups #1-7 and #9 as DUT shall detect incoming LFPS continuously
 - LFPS appearance for setup #8 as DUT shall not detect incoming LFPS
6. Repeat steps 3-5 for each setup listed in table below
7. Repeat the test for all remaining USB4 Receiver Lanes

Setup #	Pass/Fail criteria
1	DUT shall detect LFPS
2	DUT shall detect LFPS
3	DUT shall detect LFPS
4	DUT shall detect LFPS
5	DUT shall detect LFPS
6	DUT shall detect LFPS
7	DUT shall detect LFPS
8	DUT shall not detect LFPS
9	DUT shall detect LFPS

5 Captive Device Transmitter Testing

- Captive Device transmitter compliance testing is defined at the output of a compliance receptacle test fixture referenced to TP3 compliance point as depicted in Figure 17
- Calibration shall be applied in cases where direct measurement is not feasible
- USB4 v2 SigTest shall be used for all GEN4 Captive Device Transmitter testing

The following sections provide detailed information on the setup and testing of the USB4 GEN4 parameters. In the event of a discrepancy, the USB4 2.0 Specification prevails.

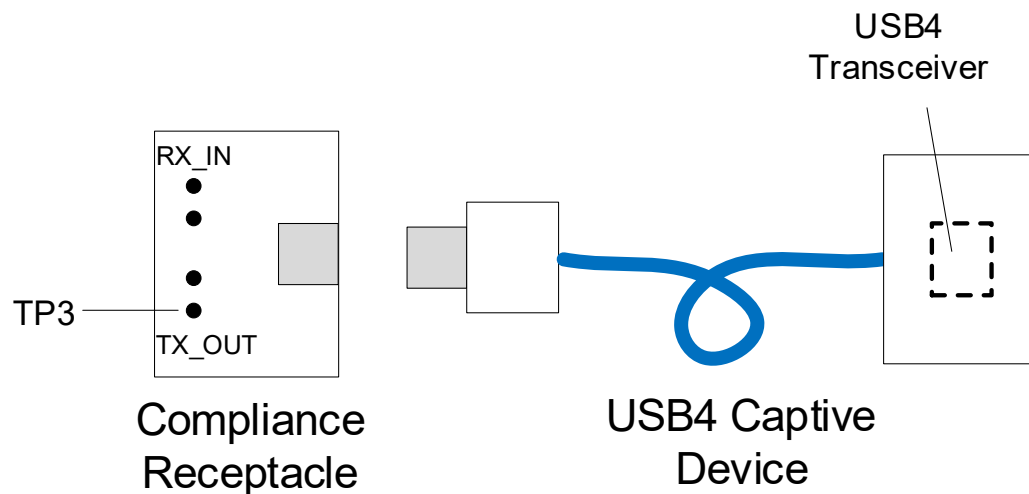


Figure 17. USB4 Captive Device TX Compliance Point Definition

5.1 Transmitter Test Setup

Figure 18 illustrates the connections to the DUT and control PC used for Transmitter testing. Cable assembly connecting DUT to Oscilloscope shall be measured using Network analyzer for further de-embedding in SigTest tool

Note:

3. Use Oscilloscope requested **Analog** Bandwidth. In case Digital Filter is used to set requested Oscilloscope Bandwidth, the usage of Brick-Wall Filter is **not** recommended
4. Before beginning any test or data acquisition, the Oscilloscope must be warmed, and calibrated. Signal vertical scaling must be optimized for maximum opening cross all tests (at least 80% of maximum scope vertical range)

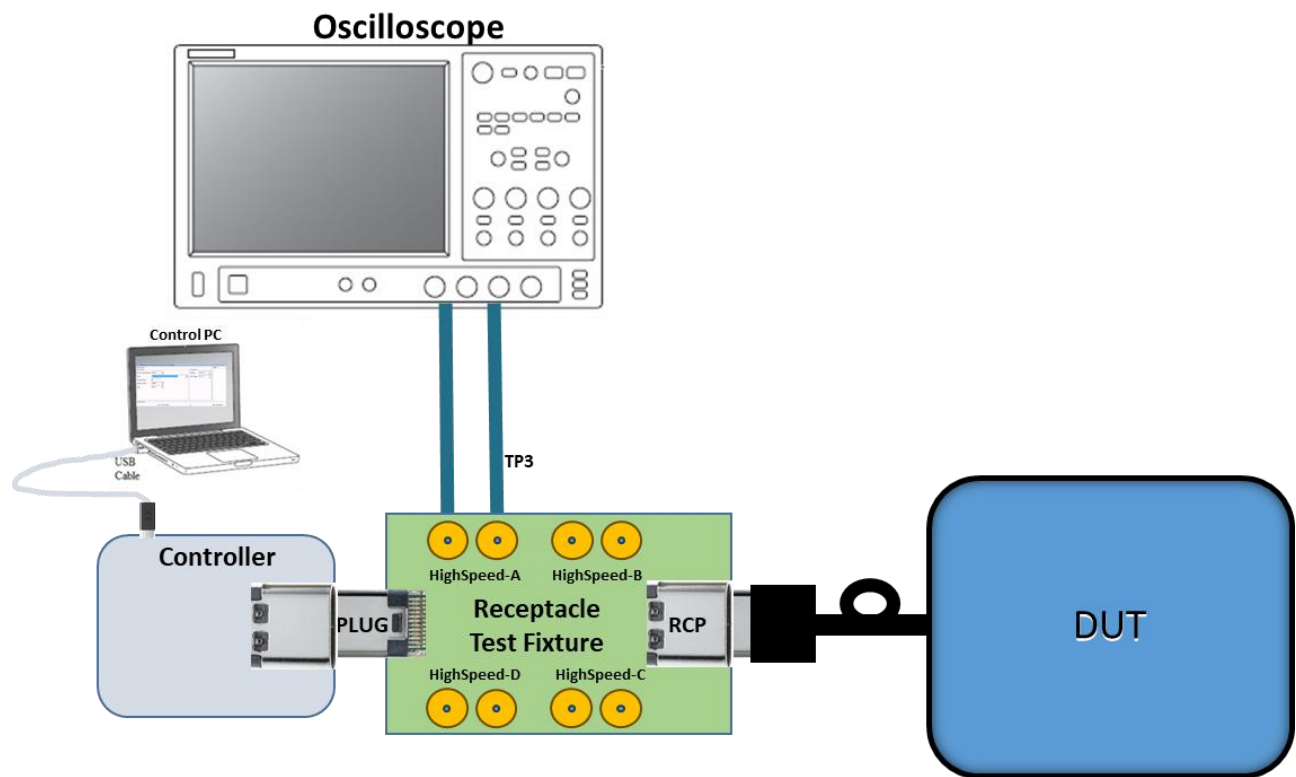


Figure 18. Transmitter TP3 Test Setup

5.2 Connecting to the DUT

1. Connect Lane under test TX_P, TX_N to the Oscilloscope.
2. Connect the Low speed signals from the USB4 test Fixture to the USB4 Micro-controller port using a USB Type-C passive cable.
3. The USB4 Micro-controller is connected to Control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT).

5.3 GEN4 Captive Device Transmitter Compliance

Note: Refer to Sections 3.2.5.2

5.3.1 GEN4 Transmitter Equalization

5.3.1.1 Reference

USB4 Specification Section 3.2.3.8, Table 3-24

Preset Number	C[-2]	C[-1]	C[0]	C[1]
0	0	0	1	0
1	0	0	0.95	-0.05
2	0	0	0.9	-0.1
3	0	0	0.85	-0.15
4	0	-0.05	0.95	0
5	0	-0.05	0.9	-0.05
6	0	-0.05	0.85	-0.1
7	0	-0.05	0.8	-0.15
8	0	-0.1	0.9	0
9	0	-0.1	0.85	-0.05
10	0	-0.1	0.8	-0.1
11	0	-0.1	0.75	-0.15
12	0	-0.15	0.85	0
13	0	-0.15	0.8	-0.05
14	0	-0.15	0.75	-0.1
15	0	-0.15	0.7	-0.15
16	0.025	-0.15	0.825	0
17	0.025	-0.15	0.775	-0.05
18	0.025	-0.15	0.725	-0.1
19	0.025	-0.15	0.675	-0.15
20	0	-0.2	0.8	0
21	0	-0.2	0.75	-0.05
22	0	-0.2	0.7	-0.1
23	0	-0.2	0.65	-0.15
24	0.025	-0.2	0.775	0
25	0.025	-0.2	0.725	-0.05
26	0.025	-0.2	0.675	-0.1
27	0.025	-0.2	0.625	-0.15
28	0.05	-0.2	0.75	0
29	0.05	-0.2	0.7	-0.05
30	0.05	-0.2	0.65	-0.1
31	0.05	-0.2	0.6	-0.15
32	0	-0.25	0.75	0
33	0	-0.25	0.7	-0.05
34	0.025	-0.25	0.725	0
35	0.025	-0.25	0.675	-0.05
36	0.05	-0.25	0.7	0
37	0.05	-0.25	0.65	-0.05

38	0.075	-0.25	0.675	0
39	0.075	-0.25	0.625	-0.05
40	0	-0.1	0.4	0
41	0	0	0.5	0

Transmit Equalization Presets Table

5.3.1.2 Requirement

For low swing mode (presets 40-41 only) the transmitter swing attenuation requirement is $6 \pm 1\text{dB}$

For both low and full swing modes the tolerance of the normalized coefficients shall be of ± 0.015 for $C[-2]$ and of ± 0.025 for $C[-1]$, $C[0]$, and $C[1]$ coefficients

5.3.1.3 Test Objective

Confirm that the transmitter equalization presets are within the USB4 2.0 Specification limits

5.3.1.4 Test Method

1. Speed GEN4. Lane under test pattern PRTS7, remaining lanes shall be activated as aggressors transmitting PRTS19 with preset#0 to 50Ω termination. SSC shall be enabled during the test
2. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
4. Capture the differential output signal with all presets one by one (total 42 waveforms). Record the Oscilloscope vertical scaling setting (voltage/div) for each preset, it will be used for further scope intrinsic noise measurement as described in Appendix C of this document
 - Preset0 is used as a reference preset for other presets analysis. Make sure to capture Preset0 and analyzed Presets at the same DUT TX conditions without power cycling in-between
5. Run SigTest tool according to User Manual documentation (refer to section 10.1)
6. Check SigTest report for pass/fail status. All presets must be passing
7. Repeat the test for all remaining USB4 Transmitter Lanes
 - In case that more than one Oscilloscope differential channel pair is used, repeat the Oscilloscope vertical scale tuning (voltage/div) and recording for each preset

Note: The de-embedding of the cable assembly connecting TP3 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed (See Appendix B for correct Network Analyzer setup)

5.3.2 GEN4 Transmitter Timing and Voltage measurement subsets

5.3.2.1 Reference

UI - USB4 Specification section 3.2.5.2 Table 3-28.

5.3.2.2 Requirement

Subset type	Symbol	Min	Max	Units
Timing Parameters subset	UI	39.0508	39.0742	ps
	SSC_DOWN_SPREAD_RANGE	0.2	0.3	%
	SSC_DOWN_SPREAD_RATE	30	33	KHz
	SSC_PHASE_DEVIATION	2.5	15.5	ns pp
	SSC_SLEW_RATE		500	ppm/ μ s
	UDJ		0.17	UI pp
	UDJ		0.075	UI pp
	UDJ_LF		0.03	UI pp
	EVEN_ODD		0.02	UI pp
Voltage Parameters subset	V_SWING	410	545	mV p
	TX_LEVELS_MISMATCH	0.975		
	TX_SNDR	34		dB
	PULSE_PEAK_NORM	-19		dB
	TX_ISI_MARGIN_CD			dB

5.3.2.3 Test Objective

Confirm that all listed above timing and voltage parameters are within USB4 2.0 Specification limits during steady-state

5.3.2.4 Test Method

1. Identify the preset and CTLE configuration that obtains the minimum DDJ by running dedicated SigTest analysis function described in section 10.2 of SigTest User Manual document

2. Run SigTest tool according to User Manual documentation using corresponding preset waveform and CTLE provided as part of waveform file name(refer to section 10.3). No new signal acquisition is required in this test
3. Check SigTest report for pass/fail status. All listed above timing and voltage parameters must be passing. In case only EVEN_ODD parameter fails, use PRBS11 pattern instead of PRTS7 and retest. If EVEN_ODD passes using PRBS11 then the overall result is Pass. If EVEN_ODD parameter still violates the specification limit then test Fails
4. Repeat the test for all remaining USB4 Transmitter Lanes

Note: scope intrinsic noise file shall be provided to SigTest with the same scope settings used for capturing the file with the selected preset configuration as described in Appendix C of this document

5.3.3 GEN4 Transmitter Frequency Variation Training measurement

Note: Skip this test if the Captive Device doesn't include Re-timers

5.3.3.1 Reference

TX_FREQ_VARIATIONS_TRAINING – USB4 Specification Table 3-28.

5.3.3.2 Requirement

TX_FREQ_VARIATIONS_TRAINING:

- $-300 \leq \text{INIT_FREQ_VARIATION} \leq 300 \text{ ppm}$
- $\text{DELTA_FREQ_200ns} \leq 600 \text{ ppm}$
- $\text{DELTA_FREQ_1000ns} \leq 900 \text{ ppm}$
- $\text{FREQ_OVERSHOOT} \leq 600 \text{ ppm}$

5.3.3.3 Test Objective

Confirm that the frequency variation during Link training is within USB4 2.0 Specification limits

5.3.3.4 Test Method

1. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
2. For emulating link training set Captive Device components as following:
 - Router shall be configured to transmit PRTS7 PAM3 pattern on all lanes. SSC modulation shall be disabled
 - Re-Timer facing USB Type-C connector shall be configured to transmit SQ224 (if supported) or SQ128 (if SQ224 is not supported) on all lanes. Re-timer shall prevent the transition to Forwarding state
3. Set Oscilloscope as following

- Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation to be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
 - Triggering on UI shrinkage, keep at least $10\mu\text{s}$ memory buffer after triggering point
4. Initiate transition to Forwarding state on the Re-Timer facing USB Type-C connector
 5. Capture the clock switch event over three stages: pre-clock switch, clock switch and post-clock switch in a single waveform as depicted in a Figure 19

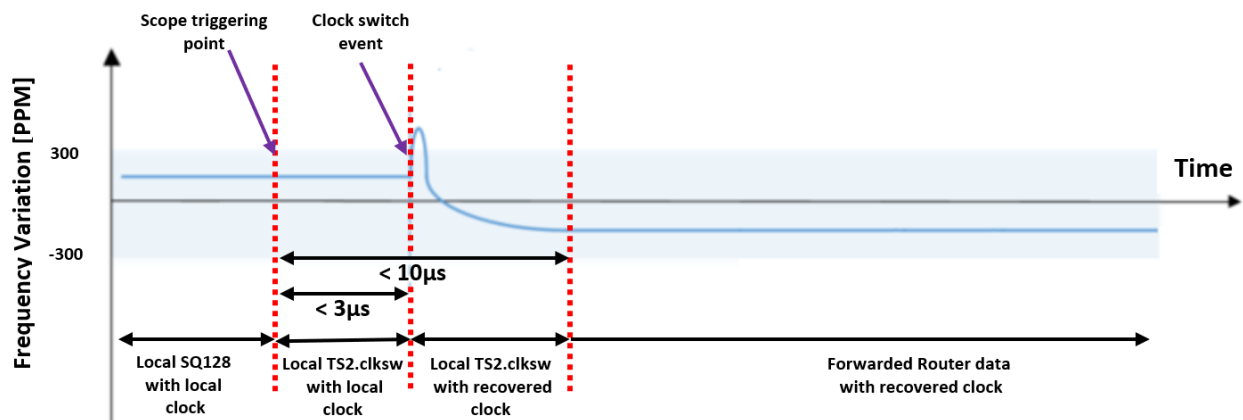


Figure 19. Frequency variation dynamics example

6. Run SigTest tool according to User Manual documentation (refer to section 10.4)
7. Check SigTest report for pass/fail status
8. Repeat above procedure 10 times. Use the worst case result as final
9. Repeat the test for all remaining USB4 Transmitter Lanes

Note: The de-embedding of the cable assembly connecting TP3 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed (See Appendix B for correct Network Analyzer setup)

5.3.4 GEN4 Transmitter Electrical Idle Voltage measurement

5.3.4.1 Reference

V_ELEC_IDLE - USB4 Specification section 3.2.5.2 Table 3-28

5.3.4.2 Requirement

$V_ELEC_IDLE \leq 20\text{mV}$.

5.3.4.3 Test Objective

Confirm that the TX peak voltage during transmit electrical idle is within USB4 2.0 Specification limits

5.3.4.4 Test Method

1. The de-embedding of the cable assembly connecting TP3 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
3. Configure DUT to Electrical Idle Mode
4. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
5. Capture the output differential signal ($V_{TX-P} - V_{TX-N}$). The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
6. Run SigTest tool according to User Manual documentation (refer to section 10.5)
7. Check SigTest report for pass/fail status
8. Repeat the test for all remaining USB4 Transmitter Lanes

5.3.5 GEN4 Transmitter AC common mode measurement

5.3.5.1 Reference

AC_CM - USB4 Specification section 3.2.5.2 Table 3-28

5.3.5.2 Requirement

$AC_CM \leq 100mVp-p$

5.3.5.3 Test Objective

Confirm that the transmitter common mode is within USB4 2.0 Specification limits

5.3.5.4 Test Method

1. The de-embedding of the cable assembly connecting TP3 compliance test point to the Oscilloscope is done by the SigTest tool. Measured cable assembly s-parameters s4p file will be used for de-embedding in SigTest tool. No additional de-embedding is needed
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80GSa/s$ while keeping acquisition record length of 500 μs
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized per preset (obtaining at least 80% of the vertical range)
3. Speed GEN4. Lane under test pattern PRTS7, remaining lanes shall be activated as aggressors transmitting PRTS19 with preset#0 to 50 Ω termination. SSC shall be enabled during the test
4. Activate Transmitter under test with maximum number of aggressor lanes configured as transmitters connected to 50 Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test and aggressors according to Appendix A)
5. Capture the output common signal $(V_{TX-P} + V_{TX-N})/2$ while transmitting with best preset as identified in section 5.3.2. The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
6. Run SigTest tool according to User Manual documentation (refer to section 10.6)
7. Check SigTest report for pass/fail status
8. Repeat the test for all remaining USB4 Transmitter Lanes

5.3.6 GEN4 Transmitter RF interference measurement

Note: This test is optional if the Captive Device doesn't include Active circuitry embedded in the tethered cable

5.3.6.1 Reference

RF_INTERFERENCE - USB4 Specification section 3.2.5.2 Table 3-28

5.3.6.2 Requirement

PWR_diff_1-14 ≤ -17dBm

PWR_comm_1-14 ≤ -47dBm

PWR_diff_36-64 ≤ -22dBm

PWR_comm_36-64 ≤ -43dBm

PWR_diff_100-140 ≤ -23dBm

PWR_comm_100-140 ≤ -44dBm

PWR_diff_149-165 ≤ -23dBm

PWR_comm_149-165 ≤ -45dBm

5.3.6.3 Test Objective

Confirm that the Captive Device Transmitter's conducted energy is within USB4 2.0 Specification limits to avoid interference to wireless systems

5.3.6.4 Test Method

1. Identify the preset configuration that obtains the minimum DDJ by running dedicated SigTest analysis function described in section 10.2 of SigTest User Manual document. Skip this step in case best preset has been identified already following section 5.3.2 completion
2. Run SigTest tool according to User Manual documentation using corresponding best preset waveform (refer to section 10.7 and 10.8). No new signal acquisition is required in this test
3. Check SigTest report for pass/fail status. All listed above Differential and Common Power parameters must be passing
4. Repeat the test for all remaining USB4 Transmitter Lanes

5.3.7 GEN4 Transmitter LFPS

5.3.7.1 Reference

USB4 Specification Section 3.4, Table 3-33

Subset type	Symbol	Min	Max	Units
Timing Parameters subset	tPeriod	20	80	ns
	tPreData	80	120	ns
	tRiseFall		4	ns
	LFPS_DUTY_CYCLE	45	55	%
Voltage Parameters subset	V_CM_AC_LFPS		100	mV p-p
	V_TX_DIFF_PP_LFPS	800	1200	mV p-p

5.3.7.2 Test Objective

Confirm that the low frequency periodic signal transmitter all listed above timing and voltage parameters are within USB4 2.0 Specification limits

Confirm that the voltage level of Electrical Idle signal during tPreData is within USB4 2.0 Specification limits as described in section 3.3.4 of this document

Confirm that the following transitions are glitch-free: Electrical Idle to LFPS, LFPS to Electrical Idle, Electrical Idle to High-Speed

5.3.7.3 Test Method

1. Transmitter under test shall be configured to transmit the following sequence:
LFPS → Electrical Idle → High Speed PRBS11 as defined in USB4 2.0 specification Section 8.3.2.2.8, table 8-76, mode 001b, Speed GEN4
2. Transmitter under test shall be activated with maximum number of aggressor lanes configured as transmitters transmitting high speed PRTS19 with preset#0 to 50Ω termination. Activate Receivers, incoming signal detection is not required (Configure Lane under test according to Appendix A.1.2 and aggressors according to Appendix A.2.3)
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of 10μs
 - No CDR, no average and no interpolation shall be used
4. The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range). LFPS shall be preceded by Electrical Idle for correct SigTest analysis
5. Run SigTest tool according to User Manual documentation (refer to section 14.2)
6. Repeat the test for all remaining USB4 Transmitter Lanes

6 Captive Device Receiver Testing

This section describes the mandatory tests required for USB4 GEN4 Captive Device Receiver compliance verification

The following sections provide detailed information on the setup and testing procedures of the USB4 GEN4 Captive Device Receiver parameters. In the event of a discrepancy, the USB4 2.0 Specification prevails.

- Calibration shall be applied in cases where direct measurement is not feasible.
- USB4 v2 SigTest shall be used for all GEN4 Captive Device Receiver testing and stress signal calibration (except TER testing)

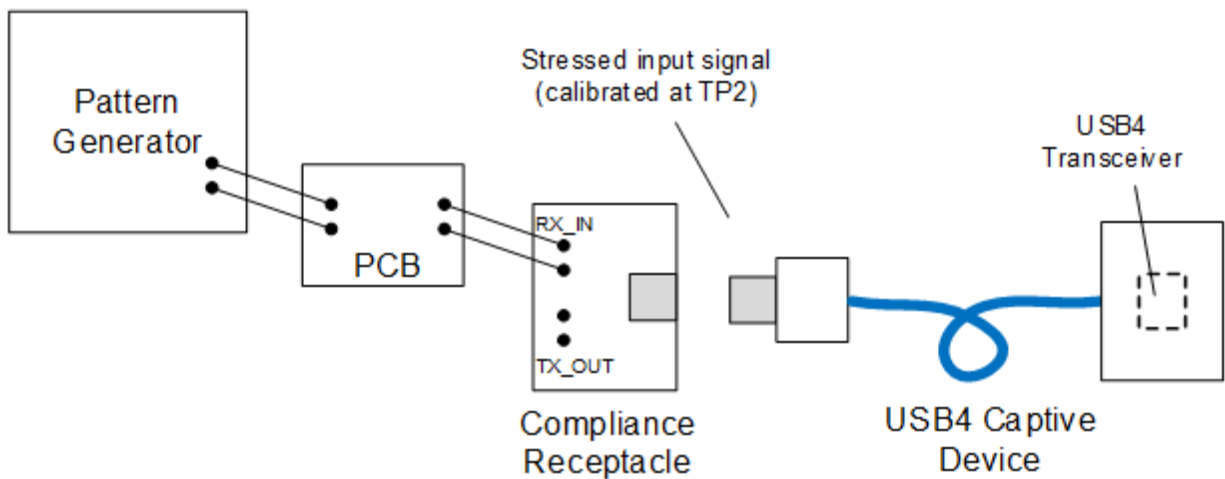


Figure 20. USB4 Captive Device RX Compliance Points Definition

A Gen 4 receiver shall operate at a Trit Error Ratio (TER) of $1E-8$ or lower without Forward Error Correction when a stressed signal is driven at its input. Tolerance testing shall be performed while all neighboring transceivers are active. There's a single test setup that shall be used for evaluating the Captive Device receiver tolerance as shown in Figure 20

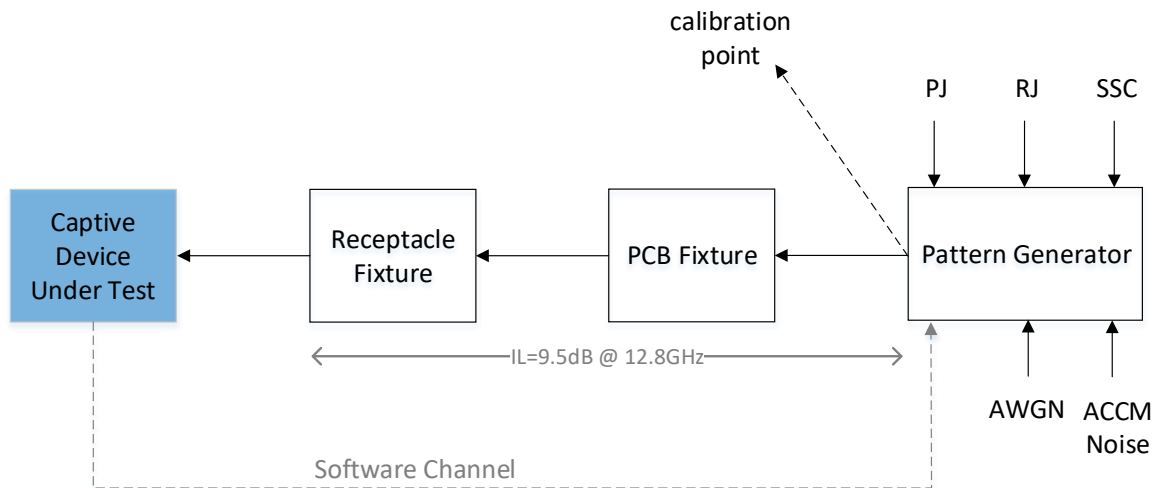


Figure 21. USB4 Captive Device RX Tolerance Test Topologies

6.1 Receiver stress signal calibration

This section describes two calibration setups

1. BERT output calibration to “worst case transmitter”
2. Test channel calibration to worst case condition

Note: Before beginning any test or data acquisition, the Generator and Scope must be warmed, calibrated, and cables de-skewed.

6.1.1 Calibration setup and BERT common settings

6.1.1.1 Calibration setup

The USB4 2.0 Specification outlines requirements for BERT output calibration as measured at the USB Type-C connector at the plug side.

Connect the calibration setup as depicted in Figure 22 below.

- Connect DC blocks at BERT data out
- Connect pair of phase matched cables from the DC blocks to the oscilloscope
- No de-embedding of phase matched cables is required

6.1.1.2 BERT common settings

BERT common settings:

- GEN4 baud rate: 25.6GB
- Test pattern: PRTS7 (PAM3)
- TX FFE preset: preset #0 (Note: Constant preset #0 setting is applicable only during calibration process. During regular TER testing DUT Receiver is allowed to request any preset defined in the spec)
- SSC:
 - SSC rate: 32kHz
 - SSC downspread deviation: 0ppm to -3000ppm
 - SSC modulation shape: triangular
- Refer to section 4.1.4.1.3.3 to confirm BERT Insertion Loss (BERT_IL) before proceeding to the subsequent calibration steps

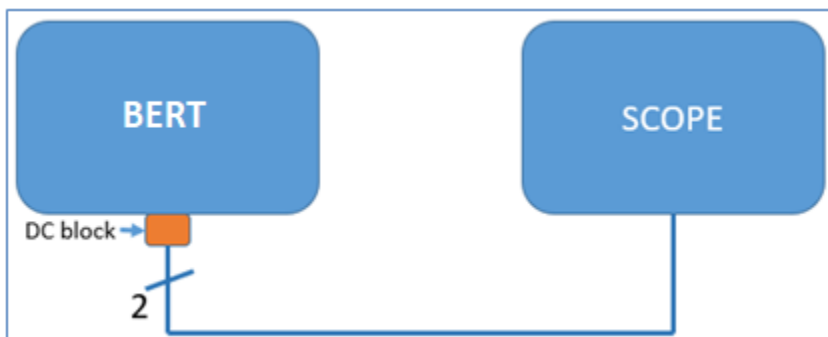


Figure 22. Receiver Calibration Setup

6.1.2 BERT output calibration

1. Construct setup as described in section 6.1.1.1 of this document
2. Configure BERT as described in section 6.1.1.2 of this document

6.1.2.1 Voltage Swing

6.1.2.1.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.1.2 Requirement

Voltage Swing – 820mV p-p \pm 15mV

Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.1.3 Test Method

1. Turn all other impairments off
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
3. Capture single ended pair of the output signal
4. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
5. Check SigTest report for Voltage Swing result
6. Adjust BERT voltage swing setting and repeat steps 4-6 until desired result is achieved

Note:

1. Record the Oscilloscope vertical scaling setting (voltage/div) of the calibrated signal
2. See Appendix D of this document on scope intrinsic noise measurement Receiver calibration procedure
3. Refer to User Manual documentation (refer to section 8.2) on scope intrinsic noise waveform usage. Scope intrinsic noise waveform shall be used for subsequent calibration steps
4. Once the Voltage Swing has been adjusted, the oscilloscope vertical scale setting shall remain constant for subsequent calibration steps

6.1.2.2 Level Mismatch

6.1.2.2.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.2.2 Requirement

Level Mismatch – 0.975 ± 0.005

Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.2.3 Test Method

1. Keep Voltage Swing as calibrated in previous step
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for Level Mismatch result
7. Adjust BERT PAM3 level ratio setting and repeat steps 5-7 until desired result is achieved

6.1.2.3 RJ

6.1.2.3.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.3.2 Requirement

RJ – 0.0085UI rms \pm 0.0005UI

Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.3.3 Test Method

1. Keep Voltage Swing, Level Mismatch as calibrated in previous steps
2. Turn all other impairments off
3. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
4. Capture single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
6. Check SigTest report for RJ result
7. Adjust BERT RJ amplitude setting and repeat steps 5-7 until desired result is achieved

6.1.2.4 SNDR

6.1.2.4.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.4.2 Requirement

SNDR – 34dB \pm 0.15dB

Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.4.3 Test Method

1. Configure differential mode sinusoidal interference frequency setting to 10GHz
2. Keep Voltage Swing, Level Mismatch, RJ as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for SNDR result
8. Adjust BERT differential mode sinusoidal interference amplitude setting and repeat steps 5-7 until desired result is achieved

Note:

Adding differential sinusoidal interference might impact on the calibrated RJ value (as calibrated in section 4.1.2.3). The added RJ is not part of the RJ calibration, thus SigTest reported RJ parameter shall be ignored from this point on

Concurrent execution of steps 6.1.2.4 and 6.1.2.5 is permissible, although strongly unrecommended

6.1.2.5 ACCM

6.1.2.5.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.5.2 Requirement

ACCM – 100mV p-p \pm 10mV

Voltage Swing [mV pk-pk]	SNDR [dB]	Level Mismatch	ACCM Noise [mV Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.5.3 Test Method

1. Configure common mode sinusoidal interference frequency setting to 400MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for ACCM result
8. Adjust BERT common mode sinusoidal interference amplitude setting and repeat steps 6-8 until desired result is achieved

6.1.2.6 PJ

6.1.2.6.1 Reference

USB4 2.0 Specification Table 3-30

6.1.2.6.2 Requirement

PJ – 0.075UI p-p \pm 0.002UI

Voltage Swing [Mv pk-pk]	SNDR [Db]	Level Mismatch	ACCM Noise [Mv Pk-Pk]	PJ [UI Pk-Pk]	RJ [UI RMS]
820	34	0.975	100	0.075	0.0085

6.1.2.6.3 Test Method

1. Configure PJ frequency to 1MHz
2. Keep Voltage Swing, Level Mismatch, RJ, SNDR, ACCM as calibrated in previous steps
3. Turn all other impairments off
4. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate \geq 80GSa/s while keeping acquisition record length of 500 μ s
 - No CDR, no average and no interpolation shall be used
5. Capture single ended pair of the output signal
6. Run SigTest tool according to User Manual documentation (refer to section 8.3.1)
7. Check SigTest report for PJ result
8. Adjust BERT PJ amplitude setting and repeat steps 6-8 until desired result is achieved
9. Repeat for remaining PJ frequencies as defined in USB4 2.0 base spec (remaining PJ frequencies 2MHz, 10MHz, 50MHz, 100MHz)
10. Save BERT setup as **Test Case** per PJ frequency

6.1.3 Test channel calibration to worst case condition

6.1.3.1 Reference

USB4 Specification section 3.2.5.2, Figure 3-39

6.1.3.2 Requirement

Calibrate Test channel defined by PCB Fixture and mated receptacle and plug test fixtures to meet following specification requirement:

Test channel insertion loss target is $(11\text{dB} - \text{BERT_IL}) @ 12.8\text{GHz} \pm 0.5\text{dB}$

Note: Follow Section 4.1.4.1 of this document for BERT_IL extraction

6.1.3.3 Test Method

1. Follow Appendix B for the Network Analyzer configuration
2. Construct a Test Channel setup as shown in Figure 23
3. Measure Test Channel Differential Insertion Loss at 12.8GHz
4. Adjust PCB Fixture insertion loss till the target is achieved
5. Save physical channel s-parameters file in s4p format
6. In case receiver asymmetric mode is supported by DUT, the asymmetric receiver lanes shall be tested using another mated test fixtures lane pair. Thus steps 1-5 shall be repeated per every mated test fixtures physical lane pair being used, calibration for symmetric lanes and additional calibration for asymmetric lanes

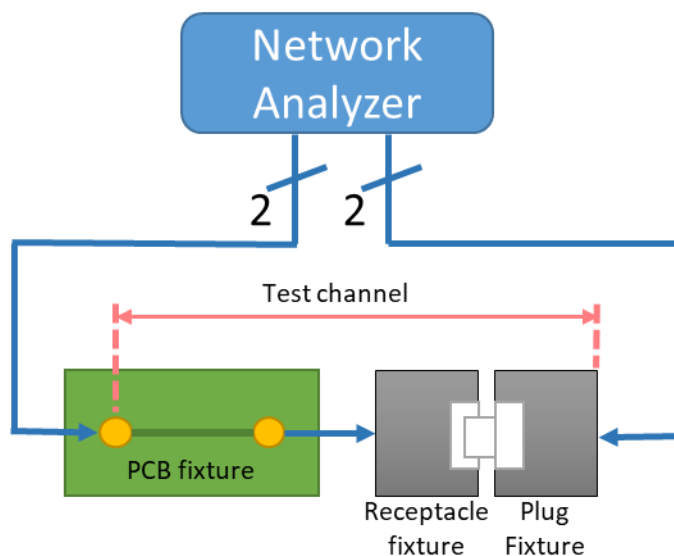


Figure 23. Test Channel measurement setup

6.2 GEN4 Receiver TER Test Procedure

Following section describes the GEN4 Receiver test procedure for Captive Device. Captive Device GEN4 receiver shall operate at a Trit Error Ratio (TER) of $1\text{E-}8$ or lower without Forward Error Correction when a stressed signal is driven at its input.

Error counter check shall be completed once per lane at single PJ frequency

It is the user's responsibility to confirm the accuracy of the BERT TXFFE coefficients with the BERT vendor, ensuring they fall within the tolerance ranges specified in section 2.2.3 of this document

6.2.1 GEN4 Receiver equalization training for TER test

6.2.1.1 Reference

USB4 Specification section 3.2.5.3.2, equalization training paragraph

6.2.1.2 Requirement

Following section describes GEN4 Receiver equalization training sequence

6.2.1.3 Test Method

1. Configure BERT to transmit PRBS11 PAM2 at GEN4 baud rate with stressed signal calibration setup without applying SSC down-spreading
2. BERT shall send ACK message once completed
3. Receiver under test shall complete equalization training #1 with PRBS11. During equalization process FFE handshake is activated
4. Receiver shall present "PAM3 without SSC ready" indication once equalization training #1 is completed
5. BERT shall switch pattern to PRTS7 PAM3 at GEN4 baud rate without applying SSC down-spreading. The switching from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document
6. BERT shall send pattern switch request ACK message once completed
7. Receiver under test shall complete equalization training #2 with PRTS7. During equalization process FFE handshake is activated
8. Receiver shall present "PAM3 with SSC ready" indication once equalization training #2 is completed
9. BERT shall switch pattern to PRTS19 PAM3 at GEN4 baud rate with Pre-Coding enabled, applying SSC down-spreading of 3000ppm. The switching from PRTS7 to PRTS19 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document. The SSC activation shall be done in a glitch-free manner such that the SSC modulation profile starts from the BERT's initial frequency as defined in section 2.2.3 of this document. SSC down-spreading and Pre-Coding enablement allowed to be asynchronous within 500usec from pattern change
10. BERT shall send pattern switch request ACK message once completed
11. Proceed to TER testing

Note: Equalization training process is part of Receiver testing and managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

6.2.2 GEN4 TER test

6.2.2.1 Reference

USB4 Specification section 3.2.5.3.2

6.2.2.2 Test setup

Construct setup as shown in Figure 24. Connect USB4 micro-controller directly to Type-C plug connector of the test fixture as shown below. USB4 Micro-controller is connected

to control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT). Use BERT assembly and Test Channel as calibrated in section 4.1.4.1 and 6.1.3 respectively of this document

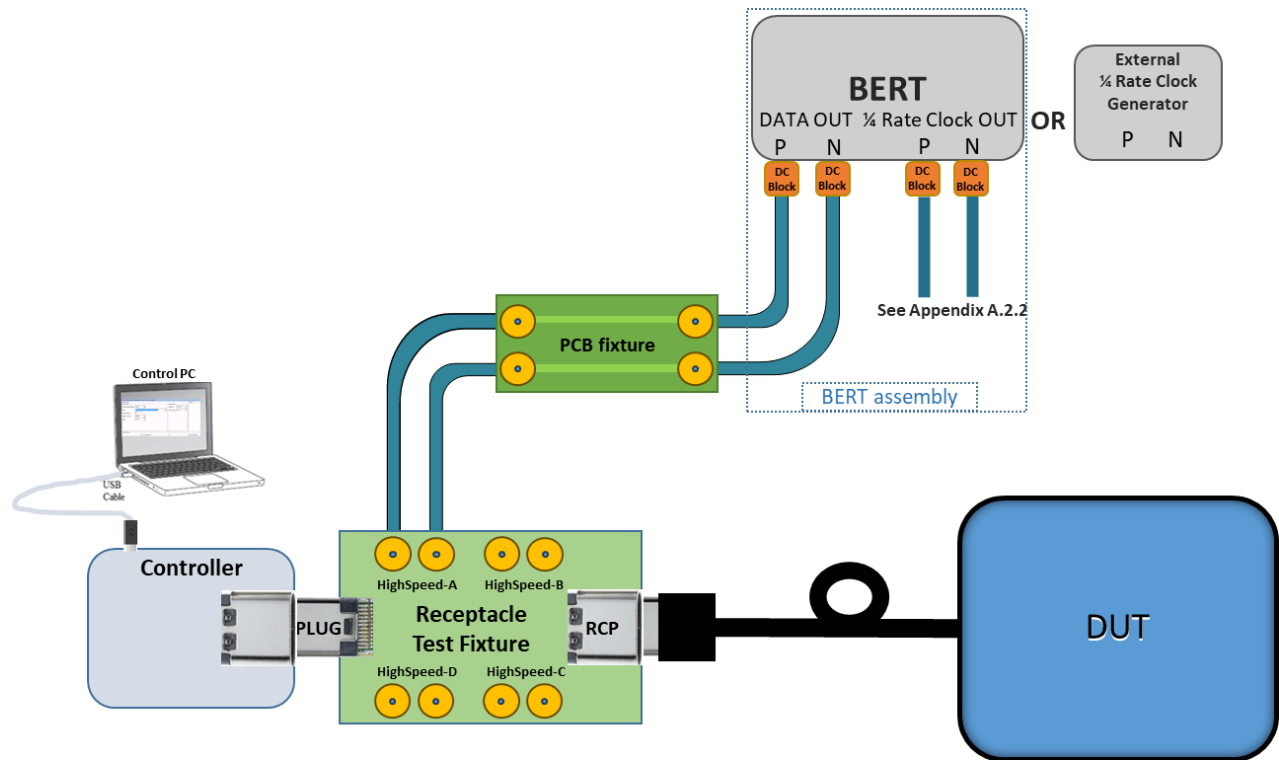


Figure 24. Captive Device Receiver Test Setup

6.2.2.3 Test Method

1. Recall Test Case calibrated setup that was saved in Section 6.1.2.6 of this document
2. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
3. Initiate Equalization training flow as described in Section 6.2.1 of this document
4. Error counter check phase (skip this section if done already for this Lane):
 - Initiate continuous random symbol error stream injection targeting TER ratio of 1E-6 using BERT
 - Start TER test
 - Wait 3sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio result is $1E-6 \pm 1.5E-7$ then Pass, else Fail
 - Error injection with reduced/disabled jitter impairments is acceptable

5. TER test phase:

- In case jitter impairments were changed during error counter check phase, repeat equalization training (steps 1-3)
 - Start TER test
 - Wait 30sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio < 1E-8 then Pass, else Fail
6. Repeat all steps above including equalization training for each PJ frequency: 1MHz, 2MHz, 10MHz, 50MHz and 100MHz
7. Repeat all steps above for each Receiver Lane. In case of asymmetric lanes use proper calibrated physical channel

Note: Receiver testing including equalization training and TER test phase is managed by ETT in interactive mode, when user is prompted on action required. Future ETT versions will include fully autonomous mode communicating with equipment directly

6.3 GEN4 Receiver Frequency Variation Training Test

6.3.1 Receiver Frequency Variation calibration

1. Construct the setup as shown in Figure 22 and following section 6.1.1
2. Recall Test Case calibrated setup for PJ 100MHz, saved in Section 6.1.2.6 of this document
3. Configure BERT to output PRTS7 with SSC down-spreading disabled
4. Construct the frequency variation dynamics as shown in Figure 25. Refer to USB4 2.0 Specification Table 3-29. Tolerance is $\pm 25\text{ppm}$ with respect to USB4 2.0 Specification targets

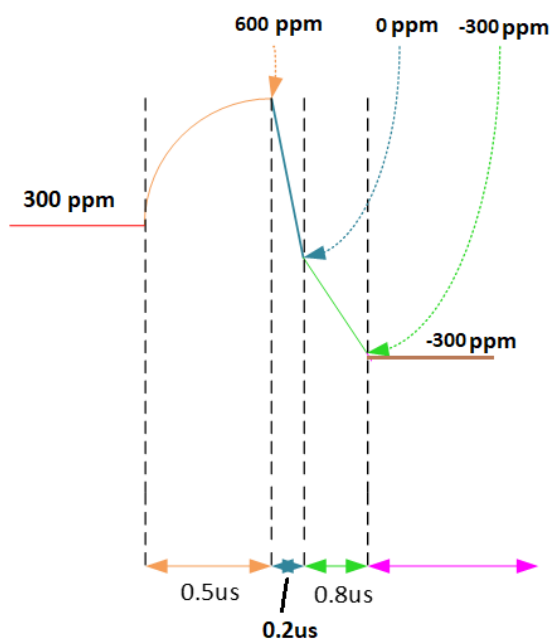


Figure 25. Frequency variation dynamics example

5. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range)
 - Set triggering capabilities to capture this event. Make sure to capture event entirely (initial frequency, clock switch and steady state after clock switch)
6. Capture the differential output signal with frequency variation dynamics
7. Run SigTest tool according to User Manual documentation (refer to section 8.4.1)
8. Check SigTest report for frequency variation parameters
9. Adjust frequency variation dynamics setting and repeat steps 6-8 until desired result is achieved
10. Save setup as **RX frequency variation Test Case**

6.3.2 Receiver equalization training for Frequency Variation test

6.3.2.1 Reference

USB4 Specification section 3.2.5.3.2

6.3.2.2 Requirement

Following section describes GEN4 Receiver equalization training sequence which applies for frequency variation test

6.3.2.3 Test Method

1. Configure BERT to transmit PRBS11 PAM2 at GEN4 baud rate with stressed signal calibration setup without applying SSC down-spreading
2. BERT shall send ACK message once completed
3. Receiver under test shall complete equalization training #1 with PRBS11. During equalization process FFE handshake is activated
4. Receiver shall present "PAM3 without SSC ready" indication once equalization training #1 is completed
5. BERT shall switch pattern to PRTS7 PAM3 at GEN4 baud rate without applying SSC down-spreading. The switching from PRBS11 to PRTS7 is asynchronous and needs to be performed in a glitch-free manner while maintaining the same jitter and noise settings as defined in section 2.2.3 of this document
6. BERT shall send pattern switch request ACK message once completed
7. Receiver under test shall complete equalization training #2 with PRTS7. During equalization process FFE handshake is activated
8. Receiver shall present "PAM3 with SSC ready" indication once equalization training #2 is completed
9. Proceed to Receiver Frequency Variation testing

Note: Receiver frequency variation testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

6.3.3 Receiver Frequency Variation test

6.3.3.1 Reference

Refer to USB4 2.0 Specification Table 3-29

Refer to Appendix F of this document for test flow diagram

6.3.3.2 Requirement

TER ratio $\leq 1\text{E-}4$

6.3.3.3 Test Objective

Confirm that the Receiver don't lose lock and record errors when frequency variation is applied.

6.3.3.4 Test Method

1. Construct the setup as shown in Figure 24, Section 6.2.2 of this document
2. Recall **RX frequency variation Test Case** saved in Section 6.3.1 of this document
3. Activate Receiver under test with maximum number of aggressor lanes configured as transmitters generating PRTS19 with preset#0 to 50 Ω termination. Activate remaining Receivers, incoming signal detection is not required (Follow Appendix A.1 for correct Lane configuration and Appendix A.2 for correct Aggressors setup activation)
4. Initiate Receiver equalization training as described in Section 6.3.2 of this document
5. TER test phase:
 - If TS2.clksw pattern is not required for this test by DUT, follow TER test TYPE I or TYPE II
 - If TS2.clksw pattern is required for this test by DUT, follow TER test TYPE II only
- 5.1. TYPE I
 - Start TER test on PRTS7
 - Send clock switch request command to BERT. BERT shall apply clock switch dynamics as calibrated in Section 4.3.1 of this document. Update query status on success in less than 1sec, Else test status is Fail
 - Wait for 2sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio $< 1\text{E-}4$ then Pass, else Fail
- 5.2. TYPE II
 - Start TER test on PRTS7 (transmitted by BERT) and send Compliance Port Operation with Pattern set to PRTS7
 - Switch to TS2.clksw pattern right after TER test start while continuing to promote PRTS7 bits in the background

- Wait 2μsec
 - Apply clock switch event within next 8μsec. BERT shall apply clock switch dynamics as calibrated in Section 6.3.1 of this document
 - Switch back to PRTS7 10μsec after switching to TS2.clksw at the exact bit position it would have been if there had been no switch to TS2.CLKSW but continuous PRTS7
 - Wait for 2sec
 - End TER test
 - Read TER ratio as reported by ETT
 - If TER ratio < 1E-4 then Pass, else Fail
6. Repeat steps 2-5 10 times
 7. Repeat all steps above for each Receiver Lane. In case of asymmetric lanes use proper calibrated physical channel

Note: Receiver frequency variation testing including equalization training and TER test phase is managed by ETT in fully autonomous mode communicating with equipment directly. User shall use ETT autonomous mode during this test

6.4 GEN4 Receiver LFPS

6.4.1 Reference

USB4 Specification Section 3.4, Table 3-33

Symbol	Min	Max	Units
V_LFPS_RX_DETECT_TH	100	300	mV p-p

6.4.2 Test Objective

Confirm that the low frequency periodic signal receiver properly detects incoming LFPS signal with voltage swing at 300mV and above

Confirm that the low frequency periodic signal receiver doesn't detect incoming LFPS signal with voltage swing at 100mV and below

Confirm that the low frequency periodic signal receiver properly detects incoming LFPS signal with each of the following calibrated to the specification limit BERT LFPS signal:

- Voltage Swing Min/Max (V_TX_DIFF_PP_LFPS)
- Period Min/Max (tPeriod)
- Duty Cycle Min/Max (LFPS_DUTY_CYCLE)
- Common mode noise Max (V_CM_AC_LFPS)

Confirm that the described above detection scenarios are stable at least within time period of 5sec

6.4.3 Calibration

1. Construct the setup as described in section 6.1.1.1 of this document
2. Set Oscilloscope as following:
 - Oscilloscope bandwidth 25GHz
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of 10 μs
 - No CDR, no average and no interpolation shall be used
3. The signal vertical scaling must be optimized (obtaining at least 80% of the vertical range). LFPS shall be preceded by Electrical Idle for correct SigTest analysis
4. Capture LFPS single ended pair of the output signal
5. Run SigTest tool according to User Manual documentation (refer to section 14.3)
6. Check SigTest report for parameter results according to setup #1 listed in table below
7. Adjust BERT settings and repeat steps 3-6 until desired parameters targets are achieved
8. Save BERT setup #1
9. Repeat steps 3-8 for each setup #2-9 listed in table below

Setup #	Swing	tPeriod	Duty Cycle	ACCM [mVpp]	Comments
---------	-------	---------	------------	-------------	----------

	[mV]	[ns]	[%]		
1	800	50	50	Off	Min swing
2	1200	50	50	Off	Max swing
3	1000	20	50	Off	Min tPeriod
4	1000	80	50	Off	Max tPeriod
5	1000	50	45	Off	Min duty cycle
6	1000	50	55	Off	Max duty cycle
7	300	50	50	Off	Above V_LFPS_RX_DETECT_TH max
8	100	50	50	Off	Below V_LFPS_RX_DETECT_TH min
9	1000	50	50	100	With ACCM

Calibration tolerance ranges:

Stress parameter	Target Value	Min	Max
Swing	800mV	800mV	810mV
Swing	1000mV	990mV	1010mV
Swing	1200mV	1190mV	1200mV
Swing	300mV	300mV	305mV
Swing	100mV	95mV	100mV
tPeriod	20ns	20ns	21ns
tPeriod	50ns	49.5ns	50.5ns
tPeriod	80ns	79ns	80ns
Duty cycle	45	45	45.5
Duty cycle	50	49.5	50.5
Duty cycle	55	54.5	55
ACCM	100mV	100mV	105mV

6.4.4 Test Setup

Construct setup as shown in Figure 26 below. Use passive cable without Emark to connect USB4 micro-controller to the DUT as shown below. USB4 Micro-controller is connected to Control PC via USB cable, running the latest USB4 SW Electrical Test Tool (ETT)

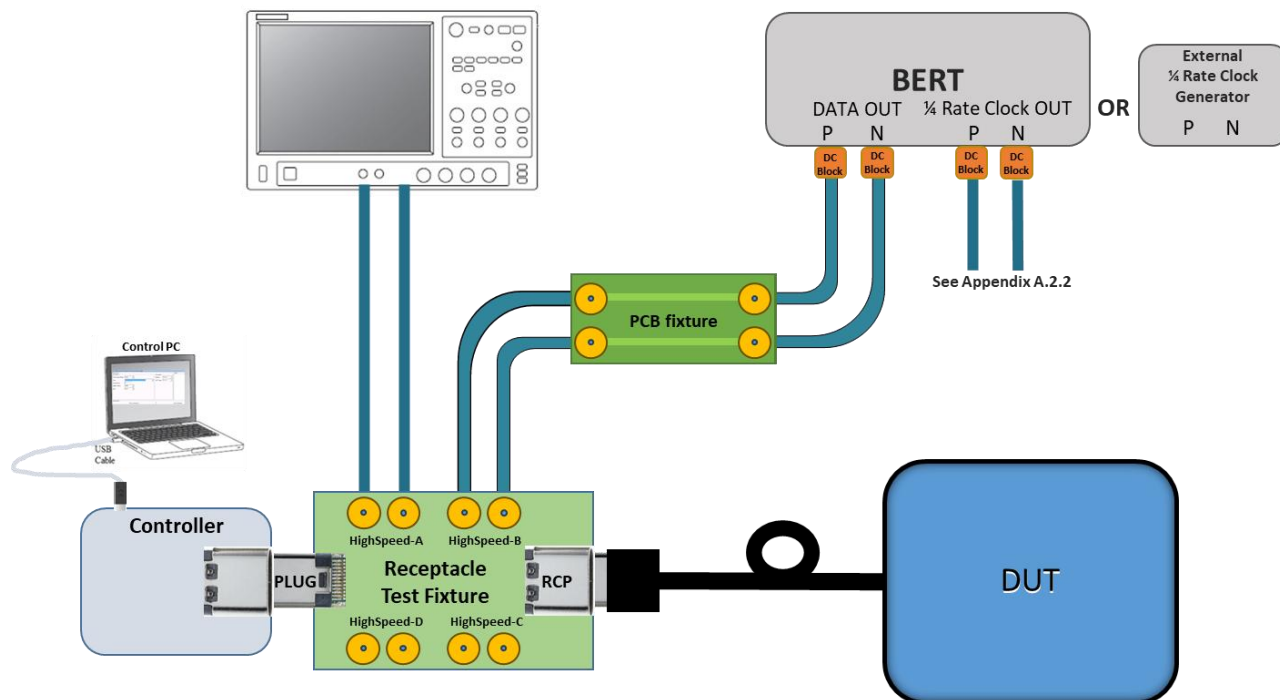


Figure 26. Receiver LFPS Test Setup

6.4.5 Test Method

1. Construct the setup as shown in Figure 26
2. Receiver under test shall be configured to detect the incoming LFPS signal as defined in USB4 2.0 specification Section 8.3.2.2.8, table 8-76, mode 011b, Speed GEN4. The detection observation shall be done through adjacent transmitter which shall transmit LFPS when it detects LFPS on receiver under test and shall move to electrical idle when not detecting LFPS on receiver under test
3. Receiver under test shall be activated with maximum number of aggressor lanes configured as transmitters transmitting high speed PRTS19 signal to 50Ω. Activate Receivers, incoming signal detection is not required (Configure Lane under test according to Appendix A.1.2 and aggressors according to Appendix A.2.4)
4. Recall calibrated setup saved in Section 6.4.3 of this document
5. Initiate LFPS Receiver test and observe LFPS Transmitter output for 5sec while triggering the scope on:
 - No signal or Electrical idle for setups #1-7 and #9 as DUT shall detect incoming LFPS continuously
 - LFPS appearance for setup #8 as DUT shall not detect incoming LFPS
6. Repeat steps 3-5 for each setup listed in table below
7. Repeat the test for all remaining USB4 Receiver Lanes

Setup #	Pass/Fail criteria

1	DUT shall detect LFPS
2	DUT shall detect LFPS
3	DUT shall detect LFPS
4	DUT shall detect LFPS
5	DUT shall detect LFPS
6	DUT shall detect LFPS
7	DUT shall detect LFPS
8	DUT shall not detect LFPS
9	DUT shall detect LFPS

Appendix A – Lane configuration and Aggressors setup

A.1 Lane configuration

A.1.1 Lane configuration for High Speed signals

This Appendix describes a DUT configuration flow to set correct Transmitter/Receiver Lane Under Test and Aggressor Lanes according to CTS requirements. Transmitter/Receiver Lane Under Test shall be tested with maximum possible neighbor lanes configured as Transmitters which depends on DUT Link Type capability.

Note: No need to physically reverse test fixture in any scenario, Lane orientation shall be configured by ETT Lane Reversal check box

Step #1:

User shall select:

1. What interface to test? (RX or TX)
2. What Link type DUT is supporting? (Choose only one option out of four listed below depends on DUT Link Type capability)
 1. Asymmetric 3xTX and 3xRX
 2. Asymmetric 3xRX only
 3. Asymmetric 3xTX only
 4. Symmetric only

Note: Symmetric link type is always supported

Step #2:

User shall follow configuration methodology described in below tables and configure ETT accordingly in order to test each Lane with correct number of aggressors. Available Lanes to be tested are marked in green.

Set ETT configurations:

1. Set Link Type
2. Set Lane Reversal check box
3. Set Lane # to be Lane Under Test


Step #3:


User shall complete Aggressors' setup configuration (as selected in step #2) and Aggressors' calibration as described in Appendix A.2

Step #4:

User shall proceed to TX/RX Lane Under Test (as selected in step #2) testing according to CTS flow

Repeat Steps 2-4 for remaining lanes

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins	
TX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+ TX0- TX2+ TX2-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	
	Option2: Asymmetric 3x RX	Symmetric	Unchecked	TX0 or TX1	TX0+ TX0- RX1+ RX1-	2
					RX0+ RX0- TX1+ TX1-	
	Option3: Asymmetric 3x TX	Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+ TX0- TX2+ TX2-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	
	Option4: Symmetric only	Symmetric	Unchecked	TX0 or TX1	TX0+ TX0- RX1+ RX1-	2
Symmetric link type is supported by default					RX0+ RX0- TX1+ TX1-	
Lane Under Test						

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane to:	Type-C connector High Speed pins	
RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX0	TX0+ TX0- TX2+ TX2-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	RX0	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	
		Asymmetric 3xRX	Unchecked	RX2	RX2+ RX2- RX1+ RX1-	
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xRX	Checked	RX2	TX0+ TX0- RX1+ RX1-	
					RX0+ RX0- RX2+ RX2-	
	Option2: Asymmetric 3x RX	Symmetric	Unchecked	RX0 or RX1	TX0+ TX0- RX1+ RX1-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xRX	Unchecked	RX2	RX2+ RX2- RX1+ RX1-	
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xRX	Checked	RX2	TX0+ TX0- RX1+ RX1-	
					RX0+ RX0- RX2+ RX2-	
	Option3: Asymmetric 3x TX	Asymmetric 3xTX	Unchecked	RX0	TX0+ TX0- TX2+ TX2-	2
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	RX0	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	
	Option4: Symmetric only	Symmetric	Unchecked	RX0 or RX1	TX0+ TX0- RX1+ RX1-	2
Symmetric link type is supported by default					RX0+ RX0- TX1+ TX1-	
Lane Under Test						

Example for TX:

Step #1:

1. TX
2. Asymmetric 3xTX & 3xRX


Step #2a:

Configure ETT to

1. Link Type: Asymmetric 3xTX
2. Lane Reversal check box: unchecked
3. Lane: TX1

Step #3a:

Proceed to TX1 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins	
TX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+ TX0- TX2+ TX2-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	


Step #2b:

Configure ETT to

- a. Link Type: Asymmetric 3xTX
- b. Lane Reversal check box: unchecked
- c. Lane: TX2

Step #3b:

Proceed to TX2 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins	
TX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+ TX0- TX2+ TX2-	4
					RX0+ RX0- TX1+ TX1-	
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+ TX0- RX1+ RX1-	
					TX2+ TX2- TX1+ TX1-	

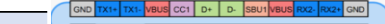
Step #2c:

Configure ETT to

- a. Link Type: Asymmetric 3xTX
- b. Lane Reversal check box: checked
- c. Lane: TX1

Step #3c:

Proceed to TX1 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration											# of Lanes to be tested
		Configure											
TX	Option1: Asymmetric 3xTX & 3x RX	Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins								4
		Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+	TX0-	TX2+		TX2-				
					RX0+	RX0-	TX1+		TX1-				
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+	TX0-	RX1+		RX1-				
								TX1+		TX1-			

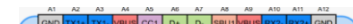
Step #2d:

Configure ETT to

- Link Type: Asymmetric 3xTX
- Lane Reversal check box: checked
- Lane: TX2

Step #3d:

Proceed to TX2 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration																# of Lanes to be tested		
		Configure																		
		Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins															
TX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	TX1 or TX2	TX0+	TX0-		TX2+	TX2-											4
					RX0+	RX0-		TX1+	TX1-											
		Asymmetric 3xTX	Checked	TX1 or TX2	TX0+	TX0-		RX1+	RX1-											
					TX2+	TX2-		TX1+	TX1-											

Overall tested 4x TX lanes

Example for RX:

Step #1:

- RX
- Asymmetric 3xTX & 3xRX

Step #2a:

Configure ETT to

- Link Type: Asymmetric 3xTX
- Lane Reversal check box: unchecked
- Lane: RX0

Step #3a:

Proceed to RX0 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration			Type-C connector High Speed pins				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane to:	TX0+	TX0-	TX2+	TX2-	
RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX0	RX0+	RX0-	TX1+	TX1-	4
		Asymmetric 3xTX	Checked	RX0	TX0+	TX0-	RX1+	RX1-	
		Asymmetric 3xRX	Unchecked	RX2	RX2+	RX2-	RX1+	RX1-	
		Asymmetric 3xRX	Checked	RX2	TX0+	TX0-	RX1+	RX1-	

Step #2b:

Configure ETT to

- Link Type: Asymmetric 3xTX
- Lane Reversal check box: checked
- Lane: RX0

Step #3b:

Proceed to RX0 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration			Type-C connector High Speed pins				# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane to:	TX0+	TX0-	TX2+	TX2-	
RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX0	RX0+	RX0-	TX1+	TX1-	4
		Asymmetric 3xTX	Checked	RX0	TX0+	TX0-	RX1+	RX1-	
		Asymmetric 3xRX	Unchecked	RX2	RX2+	RX2-	RX1+	RX1-	
		Asymmetric 3xRX	Checked	RX2	TX0+	TX0-	RX1+	RX1-	

Step #2c:

Configure ETT to

- Link Type: Asymmetric 3xRX
- Lane Reversal check box: unchecked
- Lane: RX2

Step #3c:

Proceed to RX2 testing, marked with red frame below

		<div><div>A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12</div><div><div>GND TX1+ TX1- VBUS CCI D+ D- SEU1 VBUS RX2+ RX2- GND</div><div>GND RX1+ RX1- VBUS SBUS2 D- D+ CC2 VBUS TX2+ TX2- GND</div><div>B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1</div></div></div>												# of Lanes to be tested
What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration			Type-C connector High Speed pins									
		Configure below parameters												
		Link Type to:	Lane Reversal CheckBox:	Lane to:										
RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX0	TX0+	TX0-		TX2+	TX2-					
					RX0+	RX0-		TX1+	TX1-					
		Asymmetric 3xTX	Checked	RX0	TX0+	TX0-		RX1+	RX1-					
					TX2+	TX2-		TX1+	TX1-					
		Asymmetric 3xRX	Unchecked	RX2	RX2+	RX2-		RX1+	RX1-					
					RX0+	RX0-		TX1+	TX1-					
		Asymmetric 3xRX	Checked	RX2	TX0+	TX0-		RX1+	RX1-					
					RX0+	RX0-		RX2+	RX2-					


Step #2d:

Configure ETT to

- Link Type: Asymmetric 3xRX
- Lane Reversal check box: checked
- Lane: RX2

Step #3d:

Proceed to RX2 testing, marked with red frame below

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration											# of Lanes to be tested		
		Configure below parameters													
		Link Type to:	Lane Reversal CheckBox:	Lane to:	Type-C connector High Speed pins										
RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX0	TX0+	TX0-		TX2+	TX2-						
					RX0+	RX0-		TX1+	TX1-						
		Asymmetric 3xTX	Checked	RX0	TX0+	TX0-		RX1+	RX1-						
					TX2+	TX2-		TX1+	TX1-						
		Asymmetric 3xRX	Unchecked	RX2	RX2+	RX2-		RX1+	RX1-						
					RX0+	RX0-		TX1+	TX1-						
		Asymmetric 3xRX	Checked	RX2	TX0+	TX0-		RX1+	RX1-						
					RX0+	RX0-		RX2+	RX2-						

Overall tested 4x RX lanes

A.1.2 Lane configuration for LFPS signals

This Appendix describes a DUT configuration flow to set correct LFPS Transmitter/Receiver Lane Under Test and Aggressor Lanes according to CTS requirements. LFPS Transmitter/Receiver Lane Under Test shall be tested with maximum possible neighbor lanes configured as Transmitters transmitting High Speed signal (PRTS19) which depends on DUT Link Type capability

Step #1:

User shall select:

3. What interface to test? (LFPS RX or LFPS TX)
4. What Link type DUT is supporting? (Choose only one option out of four listed below depends on DUT Link Type capability)
 5. Asymmetric 3xTX and 3xRX
 6. Asymmetric 3xRX only
 7. Asymmetric 3xTX only
 8. Symmetric only

Note: Symmetric link type is always supported

Step #2:

User shall follow configuration methodology described in below tables and configure ETT accordingly in order to test each Lane with correct number of aggressors. Available Lanes to be tested are marked in green.

Set ETT configurations:

4. Set Link Type
5. Set Lane Reversal check box
6. Set Lane # to be Lane Under Test


Step #3:


User shall complete Aggressors' setup configuration (as selected in step #2) and Aggressors' calibration as described in Appendix A.2.5

Step #4:

User shall proceed to LFPS TX/RX Lane Under Test (as selected in step #2) testing according to CTS flow

Repeat Steps 2-4 for remaining lanes

What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration															# of Lanes to be tested
		Link Type to:	Lane Reversal CheckBox:	Lane	Type-C connector High Speed pins												
TX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	TX2	TX0+	TX0-		TX2+	TX2-						4		
					RX0+	RX0-		TX1+	TX1-								
		Asymmetric 3xTX	Checked	TX2	TX0+	TX0-					RX1+	RX1-					
					TX2+	TX2-				TX1+	TX1-						
		Asymmetric 3xRX	Unchecked	TX1	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
		Asymmetric 3xRX	Checked	TX1	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
	Option2: Asymmetric 3x RX	Asymmetric 3xRX	Unchecked	TX1	TX0+	TX0-				RX1+	RX1-			2			
					RX0+	RX0-				TX1+	TX1-						
		Asymmetric 3xRX	Checked	TX1	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
	Option3: Asymmetric 3x TX	Asymmetric 3xTX	Unchecked	TX2	TX0+	TX0-				TX2+	TX2-			4			
					RX0+	RX0-				TX1+	TX1-						
		Asymmetric 3xTX	Checked	TX2	TX0+	TX0-				RX1+	RX1-						
					TX2+	TX2-				TX1+	TX1-						
		Symmetric	Unchecked	TX0	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
		Symmetric	Checked	TX0	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
	Option4: Symmetric only	Symmetric	Unchecked	TX0	TX0+	TX0-				RX1+	RX1-			2			
					RX0+	RX0-				TX1+	TX1-						
		Symmetric	Checked	TX0	TX0+	TX0-				RX1+	RX1-						
					RX0+	RX0-				TX1+	TX1-						
Symmetric link type is supported by default																	
Lane Under Test	Aggressor Transmitter																

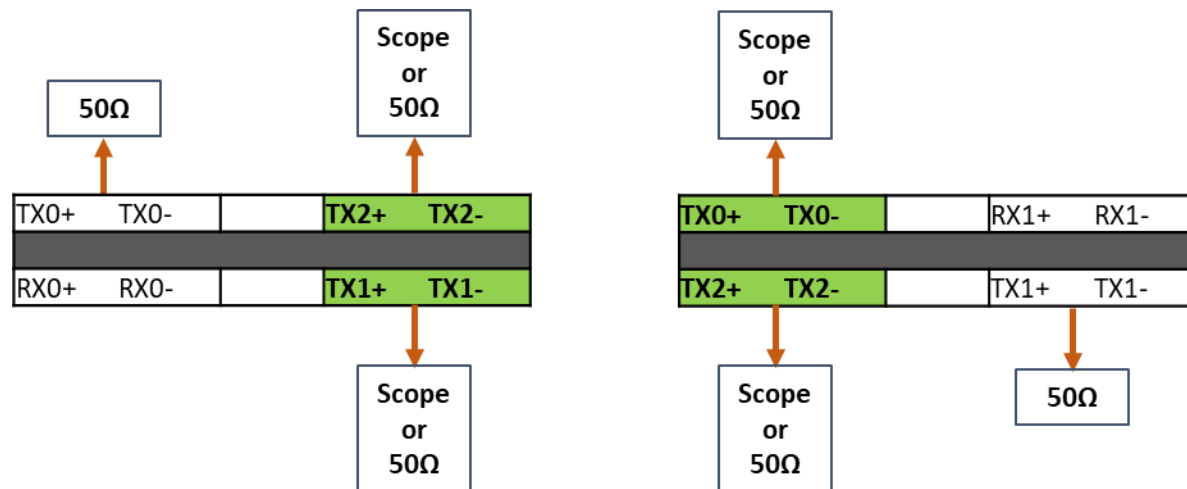
What is tested? RX or TX?	What Link type DUT is supporting? (Select one option out of four)	ETT configuration													# of Lanes to be tested																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																
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RX	Option1: Asymmetric 3xTX & 3x RX	Asymmetric 3xTX	Unchecked	RX1	TX0+	TX0-																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																									</

A.2 Aggressors setup

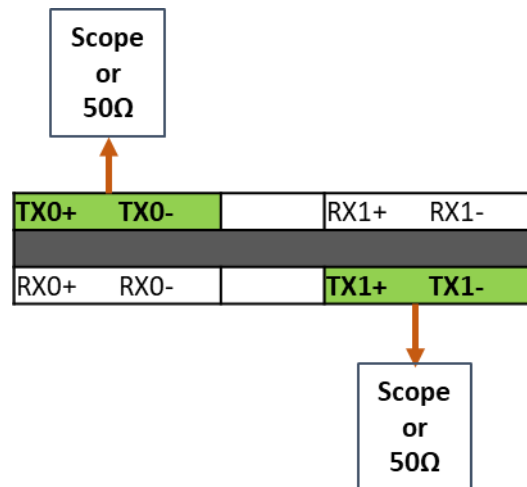
This Appendix describes an Aggressors configuration and setup for Transmitter/Receiver Lane Under Test. Transmitter/Receiver Lane Under Test shall be tested with maximum possible neighbor lanes configured as Transmitters (See section A.2.6 on aggressor signal check) which depends on DUT Link Type capability. In addition Receiver Lane Under Test shall be tested with quarter rate clock applied to other Receiver lanes, unless specified otherwise

A.2.1 Aggressors setup during TX testing

Link Type: Asymmetric 3x TX



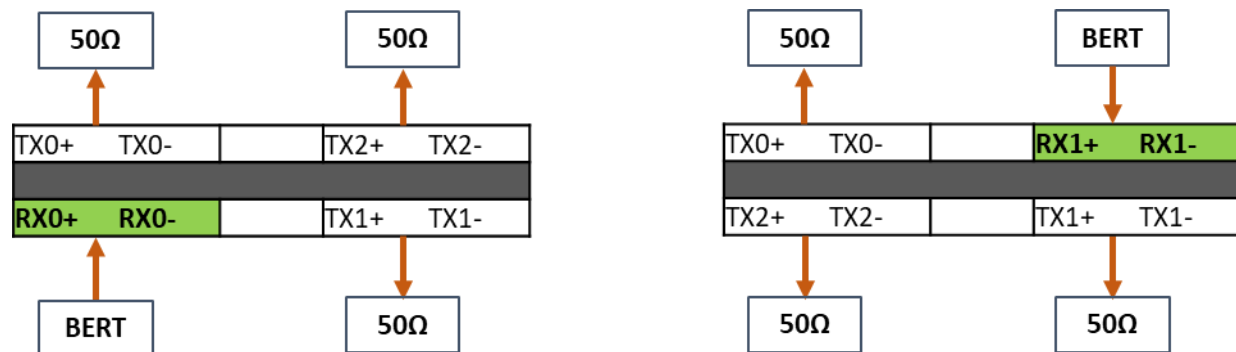
Link Type: Symmetric



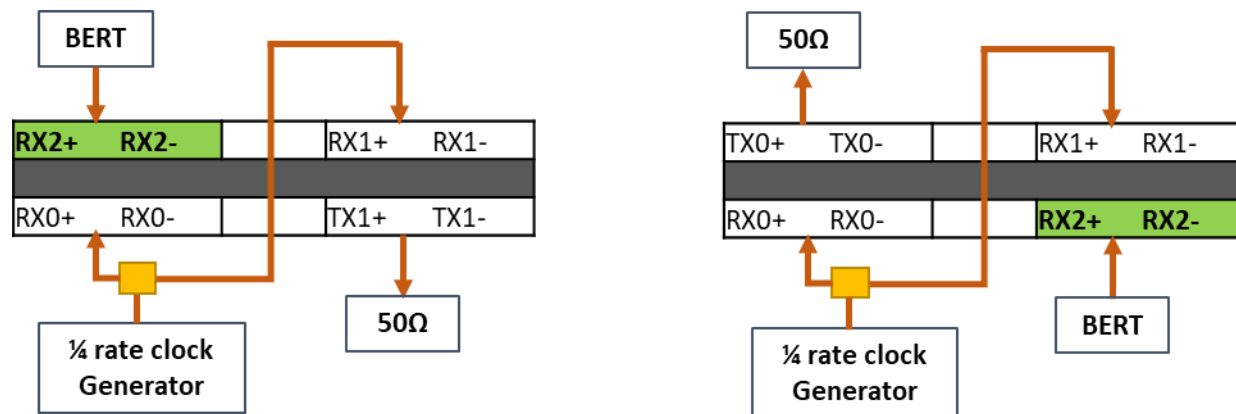
Note: Applying aggressors to Receiver lanes is not required during Transmitter testing

A.2.2 Aggressors setup during RX testing

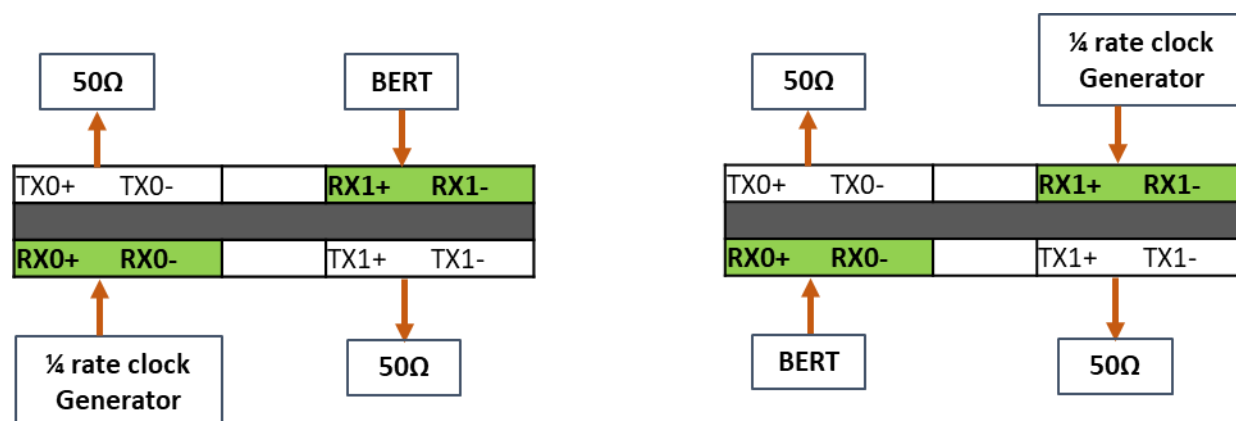
Link Type: Asymmetric 3x TX



Link Type: Asymmetric 3x RX

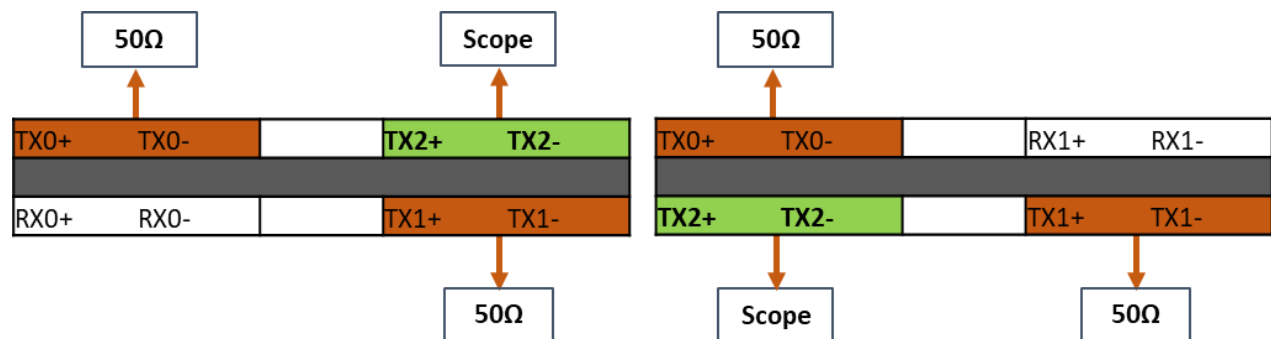


Link Type: Symmetric

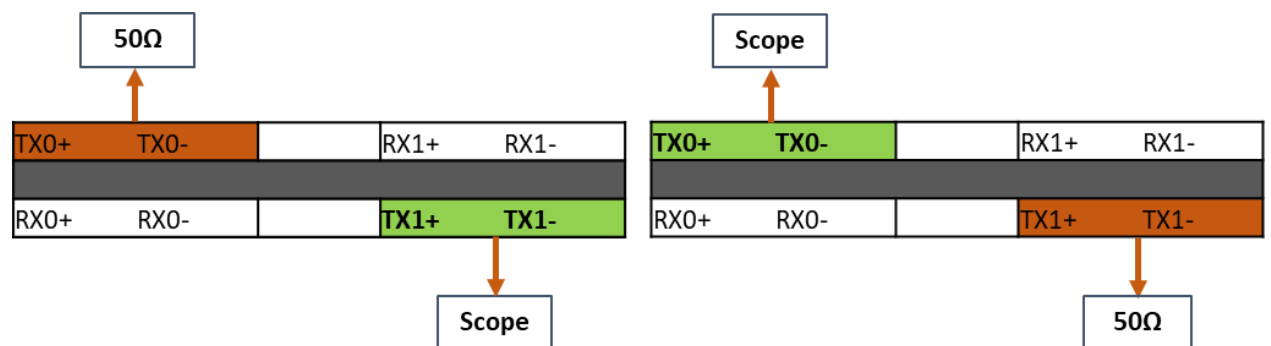


A.2.3 Aggressors setup during TX LFPS testing

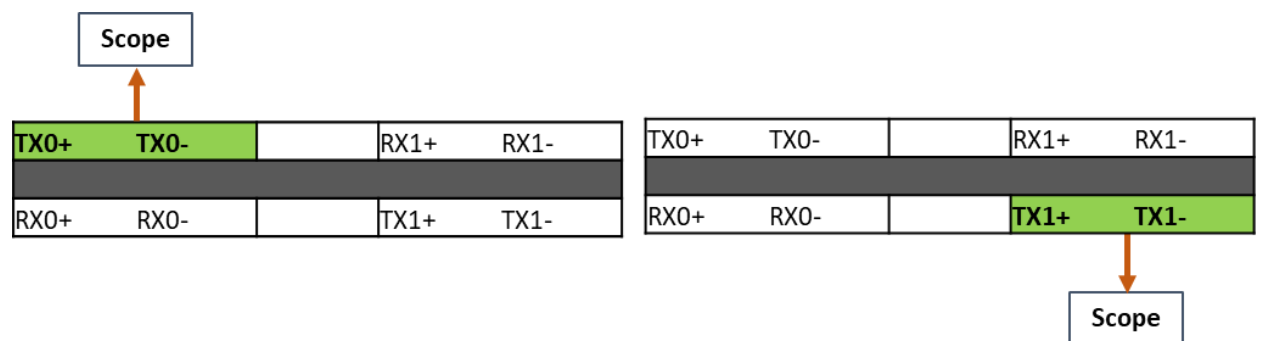
Link Type: Asymmetric 3x TX



Link Type: Asymmetric 3x RX



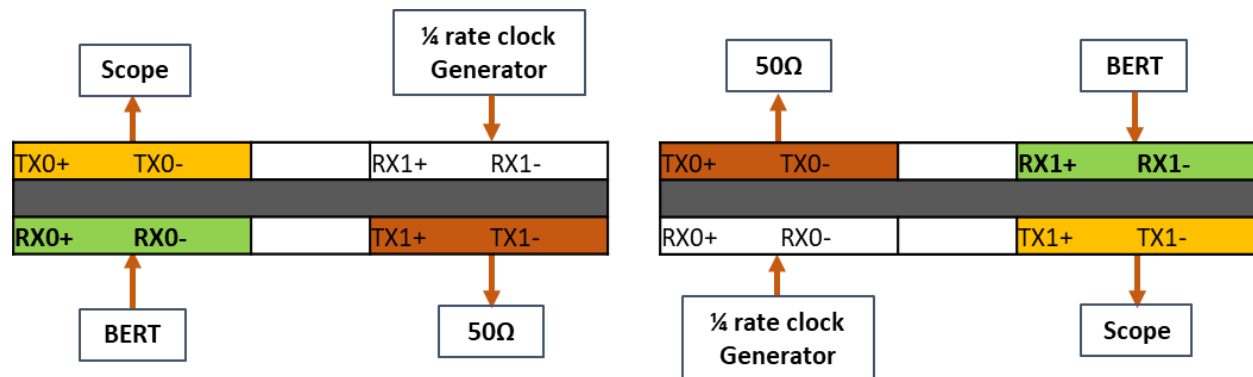
Link Type: Symmetric



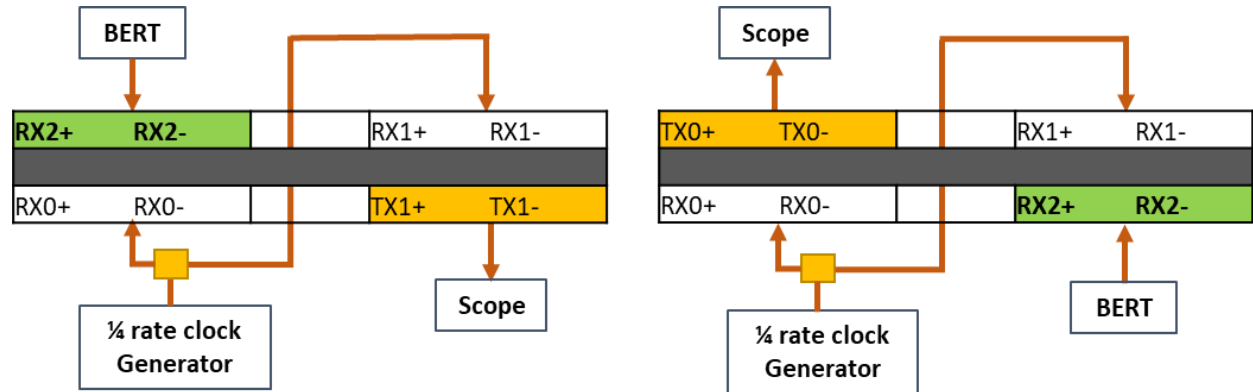
Note: Applying aggressors to Receiver lanes is not required during Transmitter testing

A.2.4 Aggressors setup during RX LFPS testing

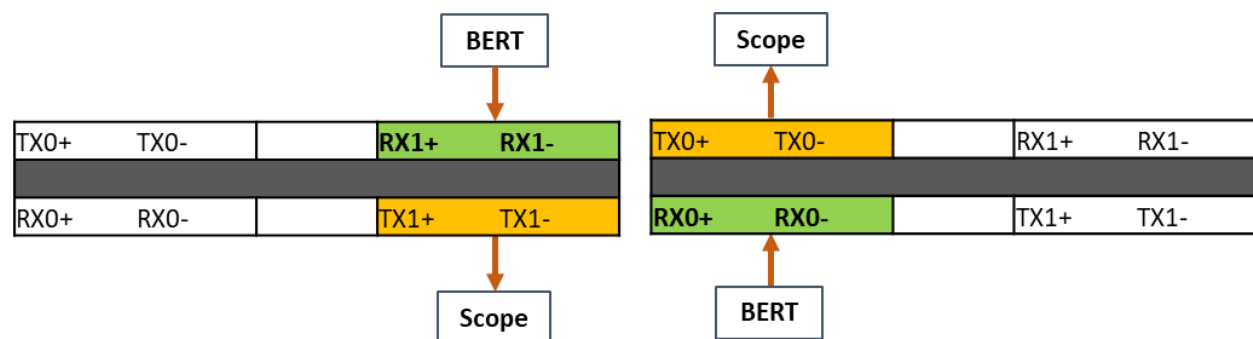
Link Type: Asymmetric 3x TX



Link Type: Asymmetric 3x RX



Link Type: Symmetric



A.2.5 Aggressor signal calibration

DUT	Interface	Test case	Amplitude
Router Assembly	RX	Case1	1090 [mV p-p]
Router Assembly	RX	Case2a/b	550 [mV p-p]
Captive Device	RX	NA	550 [mV p-p]
Router Assembly	TX		
Captive Device	TX		

Note: ¼ rate clock is 6.4GHz

Note: Amplitude calibration tolerance range $\pm 5\text{mV}$

Note: Run SigTest tool according to User Manual documentation (refer to section 8.6)

A.2.6 Aggressor signal check

Transmitter aggressor lanes shall transmit PRTS19 with preset#0 to 50 termination while keeping VSWING within the specification defined in section 3.3.2.2 or 5.3.2.2 of this document. Run SigTest tool according to User Manual documentation (refer to section 10 for Router Assembly)

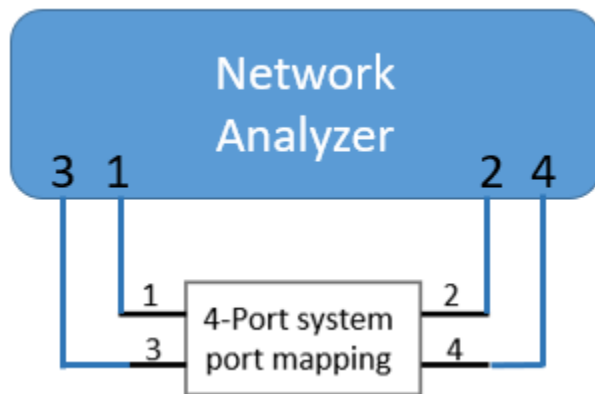
Appendix B – Network Analyzer configuration

B.1 Setup setting

- Standard class (Single Ended)
- Frequency range of 10MHz to 20GHz
- IF BW of 1KHz
- At least 2000 points
- Save s-parameter file in Normal mode (Single Ended)

B.2 4-Port mapping convention

4-Port system shall be connected as shown in figure



Network analyzer ports 1-3 shall be connected to differential input of 4-Port system
Network analyzer ports 2-4 shall be connected to differential output of 4-Port system
In case Differential input P connected to Port1 connect Differential output P to Port2
In case Differential input P connected to Port3 connect Differential output P to Port4

Appendix C – Scope Intrinsic Noise measurement for Transmitter

C.1 Requirement

Scope intrinsic noise shall be compensated in Transmitter Timing and Voltage measurement subset test as described in section 3.3.2 of this document

C.2 Test Objective

Scope intrinsic noise shall be measured using the same Oscilloscope vertical scaling as it captured for the best preset during Transmitter Equalization test described in section 3.3.1 of this document. The best preset definition is the preset with lowest DDJ as reported in SigTest Transmitter Equalization test

C.3 Test Method

1. Disconnect any cable from Oscilloscope channels
2. Connect 50ohm termination to channels used for preset acquisition
3. Set Oscilloscope as following:
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - **Oscilloscope vertical scaling of the best preset**
4. Save as **scope_intrinsic_noise.bin/trc/wfm** file name

Appendix D – Scope Intrinsic Noise measurement for Receiver calibration

D.1 Requirement

Scope intrinsic noise shall be compensated in Receiver calibration procedures as described in sections 4.1.2 and 4.1.3 of this document

D.2 Test Objective

Scope intrinsic noise shall be measured in single ended mode using the same Oscilloscope vertical scaling as it captured for the final Voltage Swing calibration value.

D.3 Test Method

5. Disconnect any cable from Oscilloscope channels
6. Connect 50ohm termination to channels used for Voltage Swing calibration
7. Set Oscilloscope as following:
 - Sampling rate $\geq 80\text{GSa/s}$ while keeping acquisition record length of $500\mu\text{s}$
 - No CDR, no average and no interpolation shall be used
 - **Oscilloscope vertical scaling final Voltage Swing calibration value**
8. Save as **scope_intrinsic_noise_p.bin/trc/wfm** and **scope_intrinsic_noise_n.bin/trc/wfm** file names

Appendix E – Mechanical

E.1 USB Type-C Receptacle Minimum Spacing

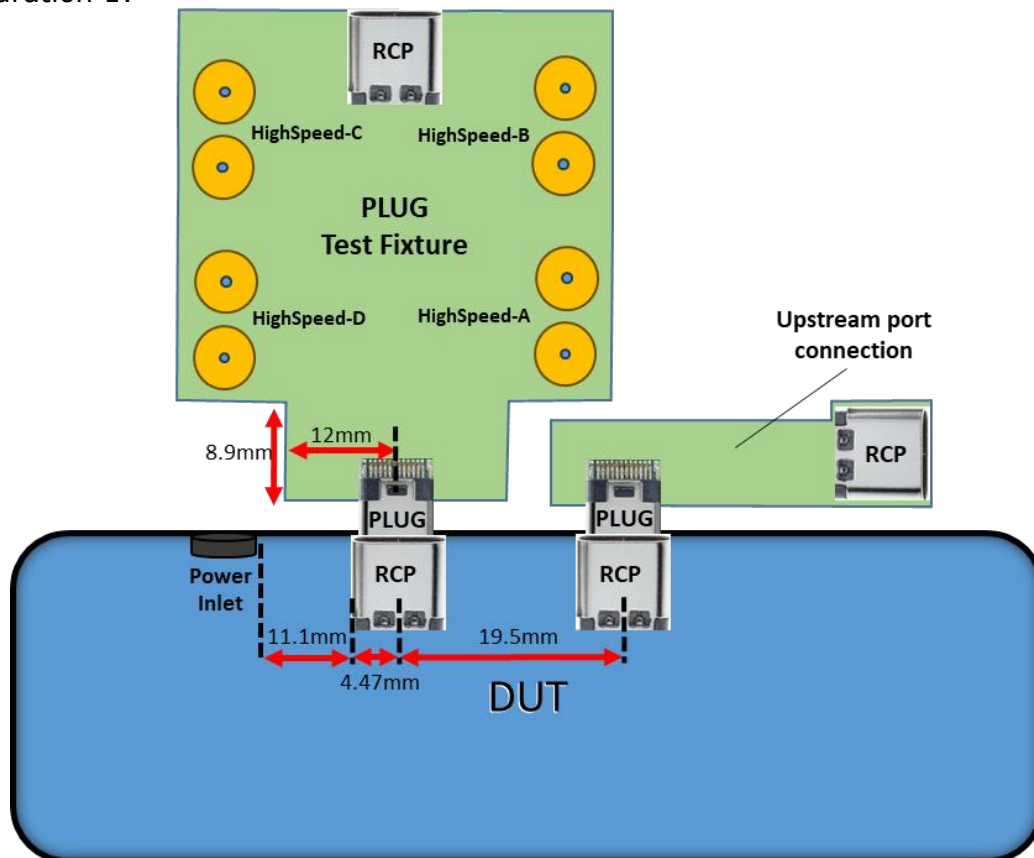
USB4 Electrical testing is performed by using Test Fixtures.

Device Under Test shall be connected to power during the testing (embedded battery or external power supply)

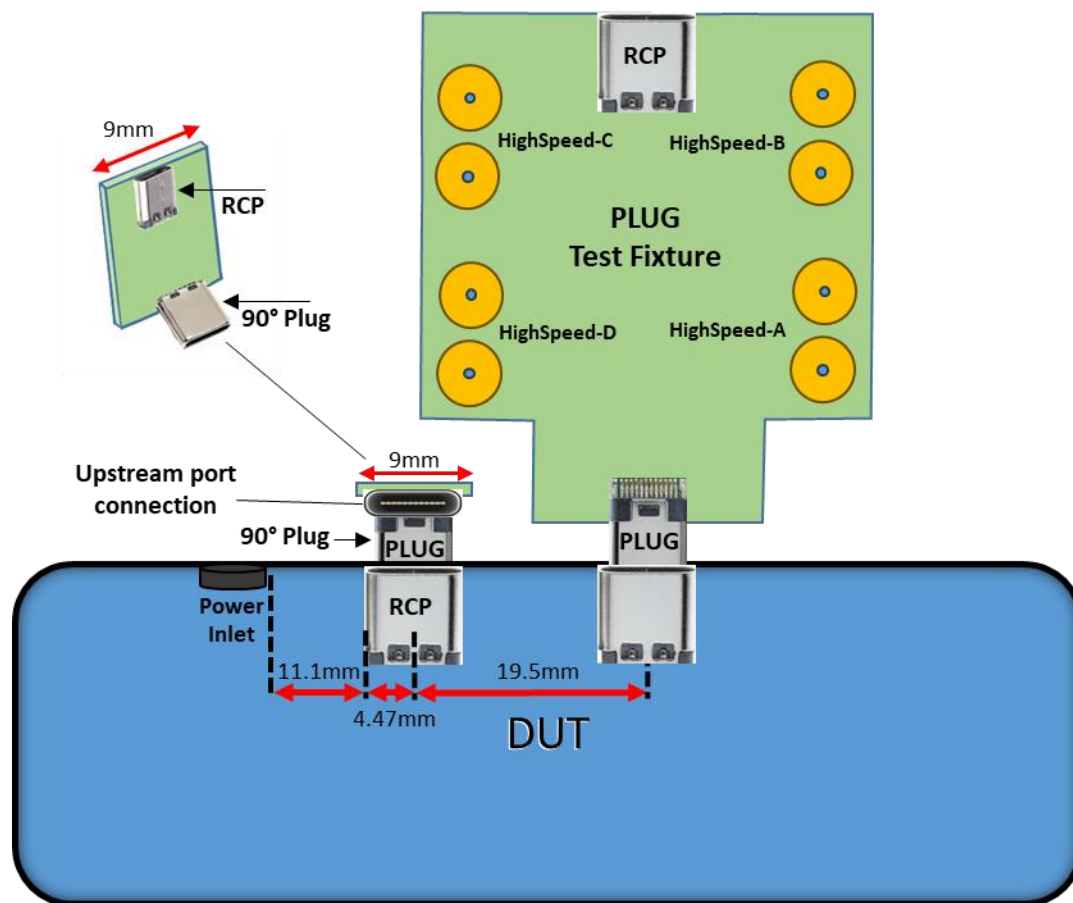
There's an option to supply charging power by test controller through certified USB4 test fixture. Pay attention on test controllers' available power capability and charging profile

In case the Device Under Test doesn't support charging through Type-C receptacle connector, power consumption isn't compatible with available power capability of test controller, or requires upstream link to be active there is a need to keep minimum spacing between USB Type-C Receptacle to the next USB Type-C connector and/or to the next Power Inlet to have enough spacing to connect power plug and/or link. The following figure illustrates the required minimum spacing

Configuration 1:

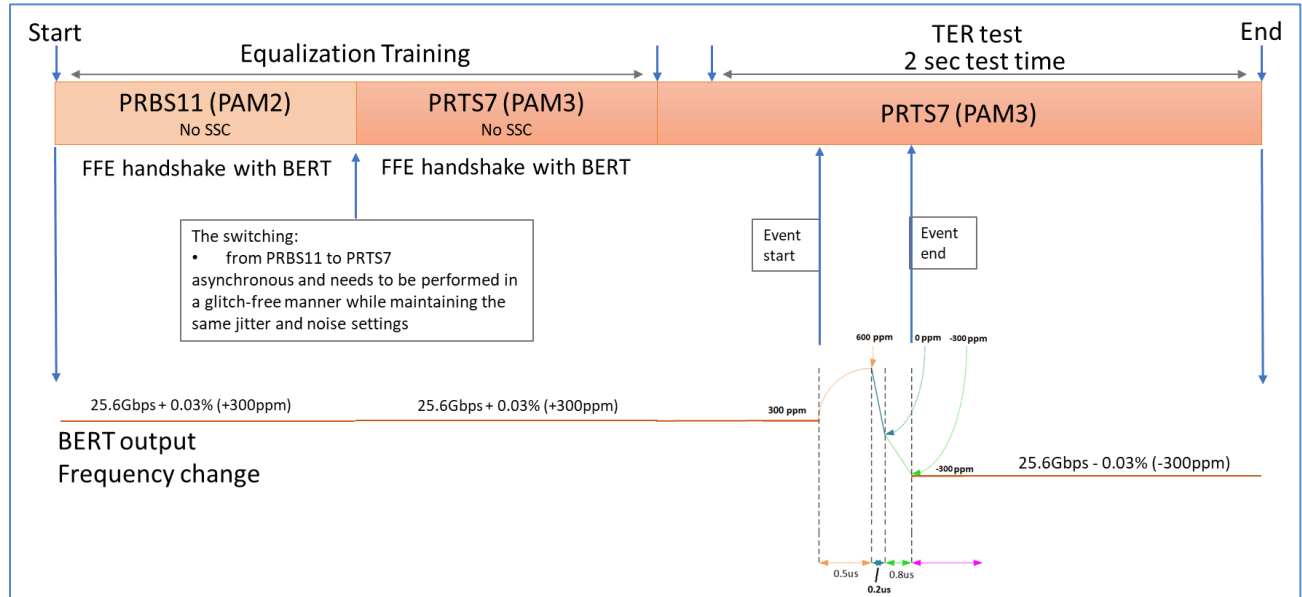


Configuration 2:



Appendix F – Receiver Frequency variation test flow diagram

1. Test Flow TYPE I



2. Test Flow TYPE II

